IEEE 9th International Symposium on Embedded Multicore/Many-core Systems-on-Chip (MCSoC-15)

Politecnico di Torino, Turin, Italy, September 23-25, 2015

September 23rd		
9:30-10:00	Registration	
10:00-10:30	Wellcome Coffee	
10:30-12:00	S1-1	S1-2
12:00-13:00	Lunch	
13:00-13:40	Dr. Roberto Zafalon (ST Microelectronics)	
13:40-15:40	S2-1	S2-2
15:40-16:00	Coffee Break	
16:00-17:30	S3-1	

September 24th		
9:00-9:30	Registration	
9:30-10:20	Prof. Luca Benini (ETH)	
10:20-10:40	Coffee Break	
10:40-12:40	S4-1	S4-2
12:40-14:10	Lunch	
14:10-15:00	Dr. Yuichi Nakamura (NEC)	
15:00-15:20	Coffee Break	
15:20-17:20	S5-1	S5-2

September 25th		
9:00-9:30	Registration	
9:30-10:20	Prof. Giovanni Demicheli (EPFL)	
10:20-10:50	Coffee Break	
10:50-12:20	S6-1	S6-2
12:20-13:50	Lunch	
13:50-14:00	Closing	

Aperitif-Dinner "Apericena"	Visit at Valentino Castle and Dinner at "Circolo dei Lettori" restaurant	Visit to "Egyptian Musem"

Wednesday, September 23rd, 2015

Start	End	Duration	Session (Room)	Details
9:30	10:00	30		Registration
10:00	10:30	30		Welcome coffee
10:30	12:00	90	S1-1	**General Issues in Many-core Programming & Programmability** Session Co-Chairs: TBD **"An Enhanced Profiling Framework for the Analysis and Development of Parallel Primitives for GPUs"** Nicola Bombieri and Federico Busato (University of Verona, Italy); Franco Fummi (Universita di Verona, Italy) **"Managing the Latency of Data-Dependent Tasks in Embedded Streaming Applications"** Xuan Khanh Do (CEA LIST, France); Stéphane Louise (CEA, LIST, France); Albert Cohen (INRIA Futurs, France) **"Measuring predictability of Nvidia's GPU schedulers: Application to the summation problem"** David Defour (University of Perpignan, France)
10:30	12:00	90	S1-2	**Methods and Tools for Efficient Architectural Design I** Session Co-Chairs: TBD **"Hierarchical Library Based Power Estimator for Versatile FPGAs"** Hao Liang (Hong Kong University of Science and Technology, Hong Kong); Yi-Chung Chen (University of Pittsburgh, USA); Wei Zhang (Hong Kong University of Science and Technology, Hong Kong); Helen Li (University of Pittsburgh, USA) **"A Scalable and Fast Microprocessor Design Space Exploration Methodology"** Lei Wang (National Unversity of Defense Technology, P.R. China); YuXing Tang (University of Defense Technology, P.R. China); Yu Deng (National University of Defense Techonology, P.R. China); Guangda Zhang (University of Manchester, United Kingdom); Feipeng Zhang (College of Finance and Statistic Hunan University, P.R. China) **"Expandable Chip Stacking Method for Many-Core Architectures Consisting of Tiny Chips"** Hiroshi Nakahara, Tomoya Oazaki and Hiroki Matsutani (Keio University, Japan); Michihiro Koibuchi (National Institute of Informatics, Japan); Hideharu Amano (Keio University, Japan)
12:00	13:00	60		Lunch
13:00	13:40	40		**Keynote speech:** Dr. Roberto Zafalon (ST Microelectronics, Italy)

13:40	15:40	120	S2-1	**Embedded Multicore/Many-core Architectures** Session Co-Chairs: TBD **"FACE: Fast and Customizable Sorting Accelerator for Heterogeneous Many-core Systems"** Ryohei Kobayashi and Kenji Kise (Tokyo Institute of Technology, Japan) **"Race-to-Finish is Energy-Inefficient for Continuous Multimedia Workloads"** Kristoffer Stokke (University of Oslo & Simula Research Laboratory, Norway); Håkon K Stensland (Simula Research Laboratory & University of Oslo, Norway); Pål Halvorsen (Simula Research Laboratory & Department of Informatics, University of Oslo, Norway); Carsten Griwodz (Simula Research Laboratory, Norway) **"Reconfigurable IBM PC Compatible for Computer Architecture Education and Research"** Eri Ogawa, Yuki Matsuda, Tomohiro Misono, Ryohei Kobayashi and Kenji Kise (Tokyo Institute of Technology, Japan) **"A CGRA-based Approach for Accelerating Convolutional Neural Networks"** Masakazu Tanomoto, Shinya Takamaeda-Yamazaki, Jun Yao and Yasuhiko Nakashima (Nara Institute of Science and Technology, Japan)
13:40	15:40	120	S2-2	**Programming Techniques for Embedded and Parallel Architectures** Session Co-Chairs: TBD **"FPU Speedup Estimation for Task Placement Optimization on Asymmetric Multicore Designs"** Alexandre Aminot, Yves Lhuillier and Andrea Castagnetti (CEA List, France); Henri-Pierre Charles (CEA, France) **"On the Load Balancing Techniques for GPU Applications Based on Prefix-scan"** Nicola Bombieri and Federico Busato (University of Verona, Italy) **"Abstracting Parallel Programming and its Analysis Towards Framework Independent Development"** Oliver Jakob Arndt and Tile Lefherz (Leibniz Universität Hannover, Institute of Microelectronic Systems, Germany); Holger Blume (Leibniz Universitaet Hannover, Germany) **"Towards Automatic Code Generation of Run-Time Power Management Systems using Formal Methods"** Asieh Salehi Fathabadi, Luis Maeda-Nunez, Michael Butler, Bashir Al-Hashimi and Geoff V Merrett (University of Southampton, United Kingdom)
15:40	16:00	20		Coffee Break

16:00	17:30	90	S3-1	**Multi-/Many-Core Applications** Session Co-Chairs: TBD **"GPU Particle Swarm Optimization Applied to Travelling Salesman Problem"** Olfa Bali (REGIM-lab University of Sfax, National Engineering School of Sfax Tunisia & TUNISIA, Tunisia); Walid Elloumi (University of Sfax, National Engineering School of Sfax Tunisia, Tunisia); Pavel Kromer (VSB - Technical University of Ostrava, Czech Republic); Adel M. Alimi (REGIM, University of Sfax, National School of Engineers, Tunisia) **"Energy-Aware Bio-signal Compressed Sensing Reconstruction: FOCUSS on the WBSN-gateway"** Daniele Bortolotti (University of Bologna, Italy); Andrea Bartolini (Università di Bologna, Italy); Mauro Mangia (University of Bologna, Italy); Riccardo Rovatti (ARCES, Italy); Gianluca Setti (University of Ferrara, Italy); Luca Benini (Unversity of Bologna, Italy) **"Top-down profiling of application specific many-core neuromorphic platforms"** Gianvito Urgese and Francesco Barchi (Politecnico Di Torino, Italy); Enrico Macii (Politecnico di Torino, Italy)

Thursday, September 24rd, 2015

Start	End	Duration	Session (Room)	Details
9:00	9:30	30		Registration
9:30	10:20	50		Keynote Speech: Prof. Luca Benini (ETH Zurich, Switzerland)
10:20	10:40	20		Coffee break
10:40	12:40	120	S4-1	**Dynamic Mechanisms for Performance Improvement** Session Co-Chairs: TBD **"Predictable Application Mapping for Manycore Real-Time and Cyber-Physical Systems"** Anil Kanduri (University of Turku, Finland); Amir-Mohammad Rahmani (University of Turku & KTH Royal Institute of Technology, Finland); Pasi Liljeberg (University of Turku, Finland); Hannu Tenhunen (Royal Institute of Technology, Sweden) **"Automatic Runtime Customization for Variability Awareness on Multicore Platforms"** Gasser Ayad and Ramakrishna Nittala (Politecnico di Torino, Italy); Romain Lemaire (CEA-LETI, France) **"Dynamic VC Organization for Efficient NoC Communication"** Masoud Oveis-Gharan and Gul N. Khan (Ryerson University, Canada) **"A performance prediction for automatic placement of heterogeneous workloads on embedded many-cores"** Nicolas Benoit (Serviware, France); Stéphane Louise (CEA, LIST, France)
10:40	12:40	120	S4-2	**Memory Management and Design** Session Co-Chairs: TBD **"Adaptive Time-Based Least Memory Intensive scheduling"** Amr Elhelw (Cairo University, Egypt); Ali A. El-Moursy (University of Sharjah, UAE); Hossam A. H. Fahmy (Cairo University, Egypt) **"Comparison of shared and private L1 data memories for an embedded MPSoC in 28nm FD-SOI"** Gregor Sievers, Julian Daberkow, Johannes Ax and Martin Flasskamp (Bielefeld University, Germany); Wayne Kelly (Queensland University of Technology, Australia); Thorsten Jungeblut, Mario Porrmann and Ulrich Rueckert (Bielefeld University, Germany) **"Lighting the Dark-Silicon 3D Chip Multi-Processors by Exploiting Heterogeneity in Cache Hierarchy"** Ashkan Sadeghi and Arghavan Asad (Iran University of Science and Technology, Iran); Mahmood Fathy (Iran University of Sci &

				Tech, Iran); Kaamran Raahemifar (Ryerson University, Canada) **"Memory Access Analysis of Many-core System with Abundant Bandwidth"** Chuan Tang and Dan Liu (National University of Defense Technology, P.R. China); Zuocheng Xing (National University of Defence Technology, P.R. China); Peng Yang, Zhe Wang and Jiang Xu (Hong Kong University of Science and Technology, P.R. China)
12:40	14:10	90		Lunch
14:10	15:00	50		Keynote Speech: Dr. Yuichi Nakamura (NEC, JP)
15:00	15:20	20		Coffee Break
15:20	17:20	120	S5-1	**Auto-Tuning for Multicore and GPU** Session Co-Chairs: TBD **"CLTune: A Generic Auto-Tuner for OpenCL Kernels"** Cedric Nugteren and Valeriu Codreanu (SURFsara HPC Centre, The Netherlands) **"Enhancement of Incremental Performance Parameter Estimation on ppOpen-AT"** Riku Murata, Jun Irie, Akihiro Fujii and Teruo Tanaka (Kogakuin University, Japan); Takahiro Katagiri (University of Tokyo & Information Technology Center, Japan) **"Improving Auto-Tuning Convergence Times with Dynamically Generated Predictive Performance Models"** James Price and Simon McIntosh-Smith (University of Bristol, United Kingdom) **"A Convergence Estimator to Auto-tune a Krylov Based Eigensolver for Large Scale Computing Systems"** France Boillod-cerneux (Lille University of Science and Technologies, France); Serge Petiton (Laboratoire d'Informatique Fondamentale de Lille, France); Christophe Calvin (CEA (French Nuclear Commision), France); Leroy Anthony Drummond (Lawrence Berkeley National Laboratory, USA) **"The Approximate Discrete Radon Transform: A Case Study in Auto-Tuning of OpenCL Implementations"** Tobias Beier (Carl Zeiss Jena GmbH, Germany); Ralf Seidler, David Neuhäuser and Hanns Martin Bücker (Friedrich Schiller University Jena, Germany)
15:20	17:20	120	S5-2	**Multicore/Many-core Interconnection Networks** Session Co-Chairs: TBD **"A Fault-tolerant Optical Switch for Highly-reliable Low-power Mesh-based Optical Networks-on-Chip"** Michael Meyer (University of Aizu, Japan); Akram Ben Ahmed and

				Abderazek Ben Abdallah (The University of Aizu, Japan) **“Hybrid Photonic NoC based on Non-blocking Photonic Switch and Light-weight Electronic Router”** Achraf Ben Ahmed (The University Of Aizu, Japan); Akram Ben Ahmed (The University of Aizu, Japan); Michael Meyer (University of Aizu, Japan) **“Communication Aware Design Method for Optical Network-on-Chip”** Martha Johanna Sepulveda Florez (INRIA, France); Sébastien Le Beux (Ecole Centrale de Lyon, Canada); Daniel Chillet, Cedric Killian and Jiating Luo (Irisa, France); Hui Li (Ecole Centrale Lyon, France); Ian O'Connor (Lyon Institute of NanoTechnology & Ecole Centrale de Lyon, France); Olivier Sentieys (INRIA, France) **“On the Design of Reliable Hybrid Wired-Wireless Network-on-Chip Architectures”** Michael Opoku Agyeman (The Chinese University of Hong Kong, Hong Kong); Wan Ji-Xiang (Xian Institute of Space Radio Technology, Hong Kong); Quoc-Tuan Vien (Middlesex University, United Kingdom); Wen Zong (The Chinese University of Hong Kong, Hong Kong); Alex Yakovlev (Newcastle University, United Kingdom); Kenneth Tong (UCL, United Kingdom); Terrence Mak (The Chinese University of Hong Kong, Hong Kong) **“3D Shared Bus Architecture Using Inductive Coupling Interconnect”** Akio Nomura, Yu Fujita, Hiroki Matsutani and Hideharu Amano (Keio University, Japan)

Friday, September 25rd, 2015

Start	End	Duration	Session (Room)	Details
9:00	9:30	30		Registration
9:30	10:20	50		Keynote Speech: Prof. Giovanni De Micheli (EPFL, Switzerland)
10:20	10:50	30		Coffee break
10:50	12:20	90	S6-1	**On-chip Communication Architectures for Multi-Core and Many-Core systems** Session Co-Chairs: TBD **"Cross By Pass-Mesh Architecture for on-Chip Communication"** Sheraz Anjum (COMSATS Institute of Information Technology, Wah Cantt, Campus, Pakistan) **"Implementation and modeling for high-performance I/O Hub used in SPARC M7 processor-based servers"** John Feehrer (Oracle Corporation, USA); Jeffry Hughes, Hugh Kurth, David Pabisz and Peter Yakutis (Oracle, USA) **"Accelerated On-Chip Communication Test Methodology Using a Novel High-Level Fault Model"** Elmira Karimi (Sharif University of Technology, Iran); Mohammad Hashem Haghbayan (University of Turku, Finland); Amir-Mohammad Rahmani (University of Turku & KTH Royal Institute of Technology, Finland); Pasi Liljeberg (University of Turku, Finland); Zainalabedin Navabi (University of Tehran, Iran)
10:50	12:20	90	S6-2	**Methods and Tools for Efficient Architectural Design II** Session Co-Chairs: TBD **"ADRENALINE: an OpenVX environment to optimize embedded vision applications on many-core accelerators"** Giuseppe Tagliavini (University of Bologna, Italy); Germain Haugou and Andrea Marongiu (Swiss Federal Institute of Technology (ETH), Switzerland); Luca Benini (University of Bologna, Italy) **"Enabling Scalable and Fine-Grained Nested Parallelism on Embedded Many-Cores"** Alessandro Capotondi (University of Bologna, Italy); Andrea Marongiu and Luca Benini (Swiss Federal Institute of Technology (ETH), Switzerland) **"The Network Performance Analysis Platform and its Application to Network Buffer Evaluation"** Yuichi Sakurai, Kenichi Shimbo and Tadanobu Toba (Hitachi, Japan); Hideki Osaka (Hitachi, Ltd., Japan)
12:20	13:50	90		Lunch
13:50	14:00	10		Closing