CALL FOR PAPERS

Special Session on On-chip Communication Architectures for Multi-Core and Many-Core systems (OCA-MC)

Recent trends in the microprocessor industry have important ramifications for the design of the next generation of computing systems. By increasing number of cores, it is possible to improve the performance while keeping the power consumption unchanged. This trend has reached the deployment stage in computing systems ranging from small ultramobile devices to large telecommunication servers. It is also expected that the number of cores in these systems rises dramatically in the near future.

On-chip communication architecture plays a crucial role to enhance the system reliability, power, and performance characteristics. In order to enable multi-core and many-core systems to provide significant performance benefits and maximize utilization of on-chip resources, many technical challenges associated with on-communication architecture should be addressed. The goal of this special session is to bring together research and industry experiences focused on architectures for on-chip communication domain.

This special session addresses all aspects of on-chip communication architecture design and test for multi-core and many-core systems. It presents new ideas in the on-chip communication field such as theory and modeling, scalable and fault tolerant design approaches and frameworks, tools and applications, analysis and comparison, design techniques and emerging implementations.

Authors are invited to submit high quality papers representing original work from both the academia and industry in (but not limited to) the following topics:

- Design space exploration and tradeoff analysis
- Novel bus and networks-on-chip architectures, including cluster interconnects
- Switching, buffering, topology, routing, and mapping algorithms
- Flow control and congestion management
- Virtualization, QoS, guaranteed throughput and on-chip real time communication
- Router microarchitecture
- Power and energy issues
- Dependable architectures
- On-chip communication architectures for the dark silicon era
- Fault tolerance and reliability issues
- Dynamic on-chip network reconfiguration
- Modeling and evaluation
- On-chip communication support for memory and cache access
- 3D on-chip architectures, emerging technologies and new design paradigms
- Timing, synchronous/asynchronous on-chip communication
- Interconnection physical link design
- Testing and verification of on-chip interconnection devices
- System prototyping
- Industrial practices and case studies

Important dates:

Paper submission: March 31, 2015
Acceptance notification: June 22, 2015
Camera ready due: June 30, 2015
Symposium: September 23-25, 2015

Session Chairs:

Hannu Tenhunen, University of Turku, Finland & Royal Institute of Technology, Sweden
Pasi Liljeberg, University of Turku, Finland
Amir-Mohammad Rahmani, University of Turku, Finland

Submission guidelines

Submissions must be in PDF and should not exceed 8 pages. The submission must adhere to the two-column IEEE style using 10 pt. fonts. The page limit includes all figures and references. All pages should be numbered. Please make use of the following link to help you in the preparation and submission of your final manuscript: http://www.computer.org/portal/web/cscps/submission

Manuscript submission

Publication

All accepted papers will be included in the proceedings of IEEE MCSoC-15 symposium.

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