MARTE and IP-XACT based approach for run-time scalable NoC

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Organization

- Introduction
- Motivation
- UML Profile for MART
- Model transformation
- Proposed approach
- Case-study
- Conclusion

Introduction

- The use of FPGA as a platform for MPSoCs is increasing from time to time

- Similarly, there is a promising progress in integrating FPGA in cloud environments for hardware acceleration

- This is due to their:
  - High performance per watt
  - Reconfigurability
  - Parallelism

- DPR is a technique that enables to dynamically modify preselected area of the FPGA at run-time and on demand.
**INTRODUCTION**

- NoC has been considered as optimal choice for FPGA based MPSoC
  - scalable
  - Increased throughput
  - Suitable to create IP chains
- A lot of works have been proposed to increase the dynamic flexibility and adaptability of the NoC

**MOTIVATION**

- How to design the NoC?
- Two possible options:
  - To write the NoC HDL using traditional handwriting method.
    - Prone to error
    - Complex
  - To automate the NoC design using high-level conceptual modeling like Unified Modeling Language (UML)
    - Complexity reduced
    - Time-to-market increased
    - Needs model transformation tools to generate the low level HDL codes

**UML PROFILE FOR MARTE**

- UML - Unified Modeling Language
  - Standardized modeling language, industry standard
- UML profile for MARTE (Modeling and Analysis of Real-Time and Embedded systems) is an extension of the UML and specifies some concepts for:
  - model-based design and analysis of real time and embedded systems
- Supports modeling of
  - Application, execution platforms, allocation
**UML Profile for MARTE**

- **MARTE** architecture is divided into four packages.
- It is modular in structure and user can choose any sub-profile needed for their design.
- For example, to design a NoC topology, the Repetitive Structure Modeling (RSM) profile can be used.

**Repetitive Structure Modeling profile**

- **Concepts**
  - **Shape**
    - To model multidimensional arrays
  - **Link topology**
    - To model the topology of the links between multidimensional arrays
    - Pattern-based regular topologies

**UML Profile for MARTE**

- **Accelerators unit**
  - 16 processors
- **Topology**
  - 4x4 grid
  - Bidirectional
    - North-south
    - East-west

**UML Profile for MARTE**

- In general, the NoC building blocks and concepts can be realized using the different MARTE profiles like:
  - Routers => MARTE profile package HW_media
  - Topology specification => MARTE profile RSM
  - Routing algorithm => MARTE state machine
  - Switching => MARTE profile enumeration
**Model Transformation**

- High-level design need to be transformed into an intermediate (system level) representation before generating the low-level HDL design (RTL level).

- The IP-XACT standard has been used for system level modeling of MP-SoC and automatic RTL generation of the target architecture.

- So, it can be used as intermediate transformation level.

**Model Transformation**

- IP-XACT standard
  - is the language-independent specification of IP meta-data.
  - Uses XML syntax to describe structure.
  - Created by SPIRIT (Structure for Packaging, Integrating and Re-using IP within Tool flows) consortium.

- Consists of several concepts/parts:
  - Component
    - Used to represent individual IPs
  - Bus Definition
    - Inter-Component communication specific resources
  - Design
    - Overall integration and connectivity of the system

- It relies on HDLs to describe IP behavior (SystemC, VHDL, ...)

**MARTE and IP-XACT Based Approach for Run-time Scalable NoC**

- MDWorkbench provides facilities to transform models and generate textual information.

- Kactus2 is a toolset for IP-XACT based SoC design.

**Case Study**

3x3 scalable NoC MARTE model
3x3 Scalable NoC MARTE model

- 2x2 Static SubNoC

- 2x1 Reconfigurable sub-column

- 1x3 Reconfigurable sub-row

- 3x3 Scalable NoC top-level
CONCLUSION

- Designing a NoC following the traditional handwriting is error prone and complex.
- The complexity can be reduced by automating the NoC design using UML/MARTE high-level modeling.
  - And increases the time-to-market
- IP-XACT is used as intermediate (system level) representation before generating the low-level HDL
- Then, the generated HDL at RTL level is used to implement the DPR based scalable NoC
- As a future work, the full system which include the NoC and IPs will be designed at high-level using MARTE

Thank You!!!

Questions?