CALL FOR PAPERS

19th IEEE International Symposium on Embedded Multicore/Many-core Systems-on (McSoC-2026)

Shanghai Jiao Tong University, Shanghai, China • Dec. 14-17, 2026

Heterogeneous Intelligence: Bridging Neuromorphic, Chiplet, Embedded, and Embodied AI Systems

2nd Round Submission Deadline: Oct 10, 2026 (HARD) | **Notification Date:** October 31, 2026 | **Camera-Ready & Registration:** November 8, 2026

Submit at: https://edas.info/N34632

The 19th IEEE MCSoC Symposium will take place in **Shanghai, China**, from **December 14–17, 2026**, sponsored by IEEE and the IEEE Computer Society TCMM. As multicore and many-core technologies advance, MCSoC provides a key forum for collaboration across academia and industry on architectures, tools, and emerging applications.

MCSoC 2026 will feature keynote talks, t**echnical tracks, and special sessions** covering heterogeneous architectures, energy-efficient computing, NoC technologies, neuromorphic and brain-inspired systems, and chiplet-based integration. Building on past editions held across Asia, Europe, and North America, the Shanghai symposium continues MCSoC's global reach.

The event will be held in a **hybrid format**, supporting both onsite and online participation. Authors are invited to submit original technical, experimental, theoretical, conceptual, or survey papers. Submission implies that at least one author will register upon acceptance.

Technical Areas

MCSoC 2026 solicits original contributions in all areas of embedded multicore and many-core systems, including architectures, design methodologies, programming models, interconnection networks, real-time systems, security, testing, low-power design, chiplet-based integration, neuromorphic and brain-inspired computing, AI acceleration, machine-learning-driven optimization, 3D integration, sustainable design, and emerging application domains. Authors should select an appropriate technical track from the detailed descriptions provided in this call when submitting their papers.

Oral Sessions

MCSoC 2026 will feature parallel technical sessions consisting exclusively of **oral presentations**. Outstanding contributions will be recognized through the **Best Paper Award** and **Best Student Paper Awards**.

Publications

MCSoC 2026 papers will undergo the standard IEEE peer-review process and follow IEEE publication guidelines. All accepted and presented papers from technical tracks, special tracks, and special sessions will be published in the **IEEE Conference Proceedings** and included in both the **IEEE Computer Society Digital Library (CSDL)** and **IEEE Xplore**.

Conference publications will also be submitted for indexing in **EI Compendex**, **Scopus**, **ISI Thomson**, and other major databases. A selection of high-impact papers may be invited to submit extended versions to affiliated journals, subject to their respective review and publication policies.

MCSoC Global Summits

- **2026 MCSoC-NeuroCore Global Summit on Neuromorphic Systems and Brain-Inspired Computing** A focused gathering of researchers advancing neuromorphic architectures, spiking neural networks, and brain-inspired computing for next-generation intelligent multicore systems.
- **2026 MCSoC-EmbodiCore Global Summit on Embodied AI and Distributed Autonomous Systems**: A dedicated forum exploring embodied intelligence, distributed autonomy, sensorimotor integration, and real-time edge systems for robotics and cyber-physical platforms.

2nd Round Submission

- Submission: ~~Sept 10~~ –> October 10, 2026 (FINAL EXTENSION)
- Notification: **October 31, 2026**
- Camera-Ready & Author Registration: **November 8, 2026**

Paper Submission System

All papers must be submitted online through EDAS at**: https://edas.info/N34632**

More Information

https://www.mcsoc-forum.org/

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Original papers solicited in the following, but not limited to, technical areas:

Programming Techniques for Embedded Multicore/Manycore SoCs: Parallel programming models, compiler support, software optimization, domain-specific languages, runtime systems, and scalable abstractions for heterogeneous manycore platforms.

Architectural Innovations in Embedded Multicore/Manycore SoCs: Novel core microarchitectures, advanced memory hierarchies, coherence mechanisms, inter-core communication schemes, and architecture-level optimizations for performance, energy, and reliability.

Design Methodologies for Embedded Multicore/Manycore SoCs: System-level design flows, HW/SW co-design, modeling and simulation frameworks, design-space exploration, and rapid prototyping methodologies for complex SoCs.

Interconnection Networks for Embedded Multicore/Manycore SoCs: NoC architectures, routing algorithms, topology optimization, congestion control, QoS-aware communication, and emerging interconnect technologies for high-bandwidth, low-latency SoCs.

Testing, Security, and Trust in Embedded Multicore/Manycore Systems: Hardware security primitives, trusted execution, fault tolerance, vulnerability analysis, side-channel mitigation, and reliability testing for secure multicore platforms.

Design Automation and Low-Power Techniques for Embedded Manycore SoCs: CAD tools, power-aware synthesis, DVFS, clock/power gating, thermal-aware design, and automated optimization flows for energy-efficient manycore architectures.

Real-Time Systems for Embedded Multicore/Manycore SoCs: Real-time scheduling, deterministic execution models, mixed-criticality systems, latency-bounded communication, and frameworks ensuring predictability in multicore real-time environments.

Operating System Platforms for Real-Time Embedded Applications: RTOS design, virtualization, hypervisors, resource management, isolation mechanisms, multicore scheduling, and OS-level support for safety-critical embedded applications.

Application Domains for Embedded Multicore/Manycore SoCs: Automotive systems, robotics, healthcare devices, industrial automation, smart infrastructure, IoT platforms, and domain-specific optimizations leveraging multicore SoCs.

Multicore SoCs for Cyber-Physical and Autonomous Systems: Sensor fusion, control loops, real-time autonomy, safety-critical processing, edge intelligence, and compute architectures enabling reliable CPS and autonomous platforms.

Hardware Acceleration of AI on Embedded Edge SoCs: AI inference engines, neural network accelerators, dataflow architectures, quantization techniques, compression strategies, and HW/SW co-design for efficient edge AI processing.

Machine Learning for Energy-Efficient and Reliable Manycore Systems: ML-based optimization, predictive reliability modeling, adaptive performance tuning, anomaly detection, and learning-driven management of power, thermal, and workload distribution.

Chiplet-Based Architectures and Design for Multicore SoCs: Modular chiplet integration, inter-chip communication fabrics, packaging technologies, interoperability standards, and scalable ecosystems for disaggregated SoC design.

Neuromorphic and Brain-Inspired Architectures for Multicore SoCs: Spiking neural networks, event-driven processing, asynchronous logic, synaptic memory structures, neuromorphic accelerators, and biologically inspired computing models.

3D Integration and Heterogeneous Design for Multicore SoCs: TSV-based stacking, interposers, logic-memory integration, photonic interconnects, thermal management, and heterogeneous integration techniques for ultra-dense SoCs.

Sustainable Design and Lifecycle Management for Multicore SoCs: Carbon-aware computing, energy harvesting, recyclable materials, lifecycle optimization, eco-efficient architectures, and sustainability-driven design methodologies for future SoCs.

Privacy-Preserving AI Acceleration on Embedded Multicore SoCs: Federated learning, homomorphic encryption, secure multiparty computation, trusted execution environments, and privacy-preserving AI acceleration techniques for embedded systems.

Formal Verification and Benchmarking of Multicore SoC Platforms: Model checking, formal proofs, simulation acceleration, standardized benchmarking, reproducible evaluation frameworks, and verification methodologies for complex multicore.

Compiler Technologies and Toolchains for Embedded Multicore SoCs: Parallelizing compilers, DSLs, toolchain co-design, intermediate representations, optimization passes for heterogeneous cores, and compiler-driven performance tuning.

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