Special Session Proposal

(IEEE MCSoC 2015)

Special session title:

General Issues in Many-core Programming & Programmability (GIM2P)

As an emerging trend in microprocessor architecture and as single-core processors' performance reached a plateau by hiting the so-called power (or heat) wall, new designs focus on augmenting the number of cores in a single processor to increase performance without increasing power consumption. This has now lead to a new category of microprocessors with several dozens computing cores on a single chip, which are usually known as "*many-core processors*". Several example are already available: Intel Xeon Phi (57 cores), Tilera GX (63 cores), Kalray MPPA-256 (256 cores), ST Micro STHORM, and even the crowd-funded 64-core Parallella Epiphany chip. The trend is expected to continue with future many-core systems with hundreds, and may be thousands of cores.

But as these processors emerge, the real issue about utilizing them and obtaining the targeted performance is the programming and programmability challenge: To harness this kind of computing power, an efficient way of doing parallel programming is required. Such a level of parallel programming is knowledgeably difficult to design to, and to manage. Therefore, this problem is a major research opportunity and a major challenge for the future of programming.

Special Session Scope

This session addresses all aspects of many-core systems programming, the issues encountered as programming existing one, and new approaches toward minimizing them. For the latter, it can range in all aspects from new programming languages or high-level software approaches to new hardware features designed to help the life of the programmer, of the compilation tools or the execution support.

Authors are invited to submit high quality papers representing original work from both the academia and industry in the following topics (but not limited to them):

- Programming models and languages for many-cores,
- Compilers for programming languages,
- Runtime generation for parallel programming on manycores,
- Architecture support for massive parallelism management,
- Enhanced communications media for CMP/manycores,

- Shared memory, data consistency models and protocols,
- Security, cryptographic systems for manycores,
- New operating systems, or dedicated OS,
- User feedback on existing manycore architectures (experimenting with programming and identifying programmability and performance issues with many-cores).

Session Chairs:

Stephane Louise, University Paris-Saclay, CEA List, France

Loic Cudennec, CEA List, France

Safae Damani, University of Bretagne-Sud, France

Tentative Program Committee:

- Akram BEN AHMED, University of Aizu, Japan
- Jeronimo CASTRILLON, CFAED / TU Dresden, Germany
- Camille COTI, Université de Paris-Nord, France
- Loïc CUDENNEC, CEA, LIST, France
- Stephan DIESTELHORST, ARM Ltd; Cambridge, UK
- Aleksandar DRAGOJEVIC, Microsoft Research Cambridge, UK
- Daniel ETIEMBLE, Université de Paris-Sud, France
- José FLICH CARDO, Universidad Politécnica de Valencia, Spain
- Bernard GOOSSENS, Université de Perpignan, France
- Vincent GRAMOLI, NICTA / University of Sydney, Australia
- Stéphane LOUISE, CEA, LIST, France
- Vania MARANGOZOVA-MARTIN, Université Joseph-Fourier Grenoble, France
- Marco MATTAVELLI, EPFL, Lausanne, Switzerland
- Maximilian ODENDAHL, Silexica / RWTH Aachen University, Germany
- Eric PETIT, Université de Versailles Saint Quentin-en-Yvelines, France
- Antoniu POP, University of Manchester, UK
- Jason RIEDY, Georgia Institute of Technology, USA
- Etienne RIVIERE, Université de Neuchâtel, Switzerland
- Thomas ROPARS, EPFL, Lausanne, Switzerland
- Martha Johanna SEPULVEDA, INRIA, École Centrale de Lyon, France
- Osamu TATEBE, AIST / University of Tsukuba, Japan

Organizers' Biographical Sketch:

Stephane Louise received his PhD from University Paris-Sud, France in 2002, and has been working at CEA LIST in two main aspects of embedded systems: Hard (dependable) Real-Time systems, and Parallel programming for embedded systems (also called "*embedded-HPC*)". On the first front, he contributed to a joined effort on the industrialization of the OASIS tools from CEA as a team collaboration with AREVA-NP that demonstrated the first general purpose Display System compliant with Nuclear Safety Standards, the QDS (Qualified Display System) product, released in 2005. On the second front, he took part in the initial design phase of Kalray's MPPA-256, the first Many-core processor designed in Europe, and was part of the team for the research, the design and implementation of parallel compilers and execution support for this Many-core. He is co-owner of several patents concerning multi- and many-core improvements. He has served as special session chair in major conferences like ICCS and contributed Program Committee of several major conferences in his area. He advised a dozen Master level and PhD students on their research works and he plans to defend his Habilitation thesis (France's Habilitation a Diriger les Recherche, HDR) at University Paris-Sud and University Paris-Saclay next April.

Loic Cudennec received his Ph.D. at the INRIA, University of Rennes 1, in the field of dynamic deployment of applications on large scale distributed systems. Some previous works include data consistency models and protocols for large-scale data sharing services and peer-to-peer performance evaluation on grid infrastructures. Since his PhD, Loïc has been working at the CEA LIST institute on parallel compilation for HPC and embedded many-core processors. He was part of a joint laboratory with the Kalray company in which several research contributions on the design of a compilation toolchain have been transferred to the development environment of the 256-core MPPA processor. He also leads a research activity on shared memory within the laboratory to explore consistency protocols and to design a compilation toolchain that takes decision on how to efficiently manage shared data online. He is also involved in several program committees, workshop organization and the advising of Master and PhD students.

Safae Dahmani received her master degree from Department of Electrical and Information Engineering at ENS Cachan. She is a PhD candidate at CEA, LIST and the University of South Brittany. She is interested in cache coherency protocols for manycores architecture. Her work was focused first on studying different techniques to manage efficiently on-chip data storage in order to address some cache coherence scalability issues. The second part of her PhD project focused on developing a multi-protocol compilation platform designed for making decisions about protocols configuration during compilation time, taking into account both the application behavior and the targeted architecture. She was involved in advising 2 master level research internships in cooperation with the LabSTICC laboratory in Lorient.