Call for papers

Fully-programmable architectures in Multi-Core and Many-Core frameworks

Nowadays, the microprocessor industry is already able to build massively parallel architectures on a single chip, and even more parallelism is expected in foreseeable devices. Such systems integrate a large number of processing elements, often heterogeneous and reconfigurable, dedicated hardware devices, and programmable gate arrays that allow a further degree of customization, even dynamic.

The opportunities carried by such an amount of computational power, however, must face the emerging challenges that may reduce the effectiveness of the technology improvements: energy efficiency, algorithm parallelization, and devices reliability are only a subset of the issues that must be taken into account.

With a dynamic system reconfiguration, devices optimized for a single application (or for an application family) can be obtained without reducing the flexibility of the platform. Processor architectures can be tailored to specific tasks, and coordinated to reduce the energy consumption; the memory architecture and the interconnect structures can be adapted to the software behavior; custom devices realized on programmable logic can alleviate the processor burden. On top of all those choices, the software must leverage the hardware features and offer a simple, flexible and effective interface to the application developers.

This special session addresses challenges and opportunities introduced by the integration of many cores, programmable logic, reconfigurable interconnects, and customizable memory architectures on the same chip.

We invite authors, from both the academia and industry, to submit original contributions that address the above and other related issues. Relevant topics include, but are not limited to:

- Energy management of multi- and many-core platforms
- Reconfigurable architectures
- Heterogeneous architectures
- FPGA architectures
- Memory architectures and data consistency
- Advances in operating systems for parallel architectures
- Static and dynamic task scheduling

Important dates:

Paper submission:	March 31, 2015
Acceptance notification:	June 22, 2015
Camera ready due:	June 30, 2015
Symposium:	September 23-25, 2015

Session Chairs:

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