

IEEE MCSoC 2021

Special Session on

Low-power Solutions for Future SoC design

Organizer: Akram Ben Ahmed (AIST, Japan)
Co-organizer: Hayate Okuhara (University of Bologna, Italy)

Nowadays, Systems-on-Chips (SoCs) are increasingly hosting several processors, memories and custom modules to satisfy the different performance requirements in high-performance and embedded applications. The increase in the number of cores, in addition to the shrinkage in the chip size, has made the power consumption one of the ultimate design challenges in such SoCs. The urge to further reduce the power consumption of SoCs has become more important with the emergence of new technologies that mainly target reduced power consumption rather than working at high frequencies. In fact, low-power processors have been required for a various Internet of Things (IoT) systems, as well as Neural Computing. The need for low-power solutions for future SoC designs has become primordial.

This special session is dedicated to present the recent architectures, techniques and methodologies for efficient low-power SoC designs. Topics of interest include, but not limited to:

- Low-power digital architectures such as power-efficient memory/cache designs, interconnections and micro architectures.
- Ultra low power chip prototyping of digital VLSI systems
- Green High-performance computing
- CAD tools and methodologies related to low power design such as power optimizations, reliability impacts on power consumption, and power modeling.
- Energy efficient software and applications including OS power scheduling and management.

Important Dates

- Abstract submission: June 25, 2021
- Full paper submission: June 30, 2021
- Acceptance notification: August 20, 2021
- Camera-ready paper: September 10, 2021

Submission

<https://edas.info/N27016>