

13th IEEE MCSoc 2019

Special Session on Traffic-aware Design for Multicore/Manycore SoCs

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The number of cores on a single SoC is ever increasing. As the core count grows, so does the amount of communications between these cores. Monitoring and adapting to this traffic can yield chips with increased performance. Congestion across the chip can also be reduced, and it becomes possible to route data in ways that avoid hotspots. These benefits often yield chips with lower power consumption compared to similarly performing chips. Monitoring and adapting to the traffic can also lead to improved thermal balance across the chip.

This special session is dedicated to present the recent architectures, techniques and algorithms for traffic-aware SoC design. The topics of interest include, but are not limited to:

- Traffic-monitoring architectures and techniques for use in routing algorithms
- Chip load balancing techniques
- Congestion-avoidance techniques
- Traffic-pattern detection
- Algorithms which adapt to traffic on the chip

Important Dates:

- Abstract Submission: April 30, 2019
- Full Paper Submission: May 7, 2019
- Acceptance Notification: June 28, 2019
- Camera-read Paper: July 21, 2019

Submission:

Please submit your paper via the IEEE MCSoc 2019 submission site.