VLSI: Key to Major Innovations

- AI
- AD
- VR
- IoT
- Big Data
- Robot
Major Risks for VLSIs

- Defective Chip Escape
- Radiation
- Aging
- Malicious Attack
- Counterfeiting
VLSI Testing: The Core Technology for Mitigating VLSI Risks

- Defective Chip Escape
- Radiation
- Aging
- Malicious Attack
- Counterfeit LSI
Scope of This Talk

Defective Chip Escape

VLSI Test
Why is VLSI Testing Necessary in Fabrication?

If all chips are good (yield = 100%)  
No Need for VLSI Testing

However, yields will never be 100% and some chips are DEFECTIVE!
Typical Defects in VLSIs

- Short
- Open
- Floating Via
- Electromigration
VLSI Testing: Basic Flow

- Test Stimuli
- Design Data
- Expected Responses
- VLSI
- Identical?
- YES
- NO
- Actual Responses
- Passing
- Failing

Design Data Flow:
1. Design
2. Fabrication
3. Test Stimuli
4. Expected Responses
5. Identical?
6. Actual Responses
7. Good or Bad?

Automatic Test Equipment
How Difficult is VLSI Testing?

VLSI Chip

Transistor Defect

Finding a missing kid from a satellite 10,000kM away from the earth.
The Ideal: *VLSI Testing as a Perfect Filter*

Manufacturer → Test (Perfect Filter) → Customer

Fabricated Chips

Good Chips → Passing Chips

Defective Chips → Failing Chips
The Reality: VLSI Testing as an Imperfect Filter

- Manufacturer
  - Good Chips
  - Defective Chips

- Test (Imperfect Filter)
  - Passing Chips
  - Failing Chips

- Customer
  - Under-Testing
  - Over-Testing

Testing Cost
Bad Chips Pass Testing  
(*shipped to the market as good chips*)

Significant Application Risk  
(*especially for mission-critical applications*)
The Impact of Over-Testing

Good Chips Fail Testing
   (discarded as bad chips)

↓

Significant Revenue Loss
   (especially for high-end chips)

Core i9-7980XE Extreme Edition
   (18 Cores / 36 Threads / 2.6GHz (Turbo: 4.2GHz) / Cash 24.75MB / 165W TDP)

1999$
The Impact of Testing Cost

Growing Testing Costs Is a Big Burden to the LSI Industry

Cost per Chip

Manufacturing Cost

Testing Cost

Year

1 Second of ATE Time = 10 US Cents

Can’t afford testing?

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Three Major Problems in VLSI Testing

- Low Quality
- Revenue Loss

Under-Testing

Test Power

Over-Testing

Testing Cost

Business Failure
Function-Mode

Low Functional Power
(Wide Use of PMS)

Test-Mode

High Test Power
(Need to Handle PMS)

Test Power Crisis
(Low Quality・High Cost・High Loss)

Growing Power Gap

Excessive Heat・Timing Failures
Higher Complexity due to PMS

Low Power Design

Power Aware Testing
Outline

1. Low-Power VLSI Design
2. Power-Aware Testing (PAT)
3. Challenges in PAT
4. Strategies for PAT
5. Future Trends
Outline

1. Low-Power VLSI Design
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Major Techniques for Low-Power VLSI Design

Avoid unnecessary operations
- Clock Gating
- Power Gating

and avoid unnecessary operation conditions
- Multiple Supply Voltages (MSV)
- Dynamic Voltage Frequency Scaling (DVFS)
- Multiple Threshold Voltages (MTV)

by using power management structures (PMS).
- Clock Gator
- Power Switch
- State Retention Register
- Level Shifter
- Isolation Cell
- Power Management Controller

Functional Power (Conventional Design)
Functional Power (Low-Power Design)
**VLSI Design: Low-Power**

Power Management Structures

- **Power Control Logic**
  - iso_enable
  - ack
  - req
  - stop_clock / save / restore
  - ack

- **Power Domain 1** (Conditionally ON)
  - Clock Gator
  - State Retention Register

- **Power Domain 2** (Always ON)
  - Clock Gator
  - Level Shifter

- **Power Domain 3** (Always ON)
  - Clock Gator

**VDD_High**

**VDD_Low**
Outline

1. Low-Power VLSI Design

2. Power-Aware Testing (PAT)

3. Challenges in PAT

4. Strategies for PAT

5. Future Trends
Impact of Low-Power Design on VLSI Testing

- **PMS-Induced**
  - High Test Cost

- **ETP-Induced**
  - Excessive Heat
  - Shift Failure
  - Capture Failure
  - Clock Stretch

**Power Management Structure (PMS)**

- Functional Power (Conventional Design)
- Functional Power (Low-Power Design)
- Test Power

**Function-Test Power Gap**

- Over-Test
- Under-Test

- Stronger Switching Activity in Test Mode
- Parallelism (faults / blocks)
- Non-Functional Test Data / Clocking
- Test Time / Cost Constraints
Growing Gap between Function Power and Test Power

SOC – Consumer Portable @ ITRS-2011

Function Power

3.5W (48M Gates) → 2.3x → 8.2W (1995M Gates)

41.7x

PMS Not Used

PMS Used

Test Power

2x (1993) → 8x (2008) → 25x-30x (2013) → 40x (2026)

Growing Gap between Function Power and Test Power

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Therefore ...

Low Power Design

Power Aware Testing
Tasks and Goals of Power-Aware Testing (PAT)

- **Low Cost**
- **PMS Test**
- **Power Management Structure**
  - Functional Power
  - Test Power (without PAT)
  - Test Power (with PAT)

**Fast & Accurate**

- Test Power Analysis
- Test Power Reduction
- Pinpoint & Safe
Outline

1. Low-Power VLSI Design
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Challenges in Power-Aware Testing

- Excessive Heat
- Shift Failure
- Capture Failure
- Clock Stretch
- PMS Test Cost
Challenges in Power-Aware Testing:

- Excessive Heat
- Shift Failure
- Capture Failure
- Clock Stretch
- PMS Test Cost

Excessive Test Power
Excessive-Test-Power-Induced Challenges: *Impact*

- **Shift**
  - Test Vector Load Started
  - Test Vector Load Completed
  - Many Shift Pulses

- **Capture**
  - Launch Capture
  - Response Capture
  - Fast Test Cycle

**Shift Power**
- Excessive Heat
- Clock Skew in Clock Tree

**Capture Power**
- Excessive Delay Increase on Long Sensitized Path
- Delay Increase on Clock Path

**Capture Failure**
- Instantaneous

**Shift Failure**
- Instantaneous

**Accumulative**
- Instantaneous

**Clock Stretch**

**(IR-Drop / L di/dt) – Induced Delay Increase and/or Clock Skew**
Excessive-Test-Power-Induced Challenges: Problems

1. Excessive Heat → Chip Damage
2. Shift Failure → Over-Testing
3. Capture Failure → Over-Testing
4. Clock Stretch → Under-Testing

Challenges:
- Chip Damage
- Over-Testing
- Under-Testing

Excessive Test Power Induced Challenges:
- Problems
Excessive-Test-Power-Induced Challenges: *Problems*

- **P1** Excessive Heat → Chip Damage
- **P2** Shift Failure
- **P3** Capture Failure → Over-Testing
- **P4** Clock Stretch → Under-Testing

IR-Drop

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IR-Drop Can Significantly Change Delay

- Same codes run on both cores.
- Right-hand core delayed by 4ns due to IR-drop.

[Franch, Huott, IBM]
Challenges in Power-Aware Testing:

- Excessive Heat
- Shift Failure
- Capture Failure
- Clock Stretch
- PMS Test Cost

Power Management Structure
Power-Management-Structure-Induced Challenge: \textit{Problem}

**Micro Power Switch Chain**
- for containing rush current

**One Power Switch**
- before DFT
  - EPWR
  - ZPWR

**Micro Power Switch Chain**
- with test wrapper implementation

**One Power Switch**
- after DFT
  - VddAlways
  - VddSwitched

---

Power-Management-Structure-Induced Challenges: Impact

- 3G mobile phone base-band chip (65nm) by ST-Ericson.
- Long test time: 36 ms for 2400 switches.
- Large additional circuitry of design for PMS test.
Outline

① Low-Power VLSI Design
② Power-Aware Testing (PAT)
③ Challenges in PAT
④ Strategies for PAT
⑤ Future Trends
Strategies for Power-Aware Testing

- Fast and Accurate Test Power Analysis
  - Excessive Heat
  - Shift Failure
  - Capture Failure
  - Clock Stretch

- Pinpoint Test Power Reduction for Safety

- Low-Cost Design / Scheduling for PMS Test
  - PMS Test Cost

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Strategies for Power-Aware Testing:

Fast and Accurate Test Power Analysis

- Excessive Heat
- Shift Failure
- Capture Failure
- Clock Stretch
Local Capture Power Analysis for Capture Failures: Method

Estimating Impact of Capture Power on LSP

Impact Area of Path P

On-Path Gate G

Aggressor Region of Gate G

Long Sensitized Path P

WSA of the Impact Area of P

N1 N2 N3 N4
N5 N6 N7 N8
N9 N10 G N11 N12
N13 N14 N15 N16
N17 N18 N19

VDD

VSS

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Local Capture Power Analysis for Capture Failures: *Reason*

Low Correlation between Path Delay and Global SA

**Maximum Frequency Determining Path**

Strategies for Power-Aware Testing:

- Excessive Heat
- Shift Failure
- Capture Failure
- Clock Stretch

Pinpoint Test Power Reduction for Safety
ATPG for Capture-Failure-Safety

Capture-Failure-Safety

Rescue & Mask
Basic Idea

Minimize the Hamming Distance between PPI and PPO

Capture Switching Activity

Combination Portion

Vector

Response

PPI

PPO

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Basic Approaches

Reduce the Number of Simultaneously-Switching FFs

Clock Control Modification

Test Vector Manipulation

In-ATPG / Post-ATPG

(Gated Clock Disabling)

Equalize D and Q

Test Vector Manipulation

In-ATPG

(Constraint-Based ATPG / X-Filling)

Post-ATPG

(Low-Capture-Power X-Filling)
ATPG for Capture-Failure-Safety

Our Method

Conventional

- Test Cube Generation w/ Dynamic Compaction
  - B

- Detection-Oriented X-Filling (Random-Fill, etc.)
  - C

Detection Bits

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<th>b</th>
<th>c</th>
<th>d</th>
<th>e</th>
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Free Bits

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Risky-Path-Impact X-Bits

- Impact Areas
  - Risky
  - lsp1

- Impact Areas
  - Risky
  - lsp2

P-I (Risky Path Checking)

- C1
  - V1

X-Restoration for Risky Paths

- C2
  - V2

X-Filling for Reducing Local LSA

P-II (Risky Path Elimination)

Remaining Risky Path Masking

- R1
  - R2

Non-Impact Change Bit Release

- V3
  - Free Bits
  - Detection Bits

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### Result

(Commercial ATPG)

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<th># of FFs</th>
<th>Max. Path Length</th>
<th># of Vectors</th>
<th>FC (%)</th>
<th>BCE (%)</th>
<th>SDQL</th>
<th># Risky Paths</th>
<th>Ave. WSAcp</th>
<th>CPU (Sec.)</th>
<th>Δ# of Vectors (%)</th>
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- Test data inflation is large.
- Risks of capture failures remain even with LCP-ATPG vectors.
**Result**

*(Our ATPG)*

Test data inflation is very small.

Impact on test quality (FC, BCE, SDQL) is negligible.

Capture-failure-safety is guaranteed.
Industry Impact

Adopted by Major EDA Companies and Applied for Testing Low-Power VLSIs in Smart Phones, Camaras, etc.
Outline

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Paradigm Shift: From Low-Power Testing to Right-Power Testing

Test Power Problems
Excessive Heat / Shift Failure / Capture Failure / Clock Stretch

Now

Low-Power Testing
Coarse-Grained

Unfocused (Global) Analysis/Reduction
No Test Power Safety Guarantee
Risk of Over-Reduction
Power Reduction Only
Risk of Test Quality Degradation
Severe Test Data Inflation

Future

Right-Power Testing
Fine-Grained

Focused (Local) Analysis/Reduction
Guaranteed Test Power Safety
No Over-Reduction
Possible Power Increase
Minimum Test Quality Impact
Minimum Test Data Inflation

(X. Wen, Proc. ETS, 2012)
Paradigm Shift: From Low-Power Testing to Right-Power Testing

Test Power Problems

Excessive Heat / Shift Failure / Capture Failure / Clock Stretch

Now

Low-Power Test

Cannon Fire

Future

Right-Power Test

Sniper Shot

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(X. Wen, Proc. ETS, 2012)
No need to consider dead areas. Hot areas must be removed by reducing local switching. Cold areas may be made “warm” by increasing local switching.

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Key Message

High Performance → Successful VLSI → Low Power

Function-Mode

Low Functional Power
(Wide Use of PMS)

Test-Mode

High Test Power
(Need to Handle PMS)

Growing Power Gap

Test Power Crisis
(Low Quality • High Cost • High Loss)

Low Power Design

Power Aware Testing

Excessive Heat • Timing Failures
Higher Complexity due to PMS

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References

The Latest Textbook on VLSI Testing

The Only Book on Power-Aware Testing