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FROM RESEARCH TO INDUSTRY

# A survey of main dataflow MoCCs for CPS design and verification

## 15th IEEE MCSoc 2022

December 19-22, 2022

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# Your speaker

- | Guillaume Roumage
- | 2<sup>nd</sup> year Ph.D. student
- | Ph.D. thesis on the dynamic reconfiguration of CPS while preserving temporal properties
- | Selma Azaiez and Stéphane Louise (both co-authors) are my advisors
- | Affiliates at University Paris-Saclay and CEA (French Alternative Energies and Atomic Energy Commission)



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I. MoCC-based design of CPS: an ADAS motivating example

II. Classification of dataflow MoCCs

III. Expressiveness hierarchy of dataflow MoCCs

IV. Conclusion



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# Motivating example: ADAS

- | An autonomous car (ADAS: Advance Driver Assistance System) has several constraints:
  - Real-time constraints (periodic execution of some components)
  - Limited resources (computation, memory)
  - Temporal constraints (latency, throughput)
  
- | How can we ensure ADAS safety without compromising the above constraints?
  - ① Model ADAS (or any CPS) with a Model of Computation and Communication
  - ② Static analysis of the CPS
  - ① + ② = **MoCC-based design of CPS**



# Motivating example: ADAS



- ADAS runs with finite memory (consistency)

- ADAS has no deadlocks (liveness)

- Real-time components fulfill their constraints



# Motivating example: ADAS

*Which DF MoCC ?*

- ADAS runs with finite memory (consistency)

- ADAS has no deadlocks (liveness)

- Real-time components fulfill their constraints

Real life system

Static analyses

**What are the differences between dataflow MoCCs? How to choose a dataflow MoCC?**

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# Classification of data flow MoCCs I

- | Synchronous Data flow and its extension : 10 DF MoCCs
  - SDF semantic ([1]) + another feature, e.g., actors auto-concurrency, multi-dimensional channel, etc.
  - HSDF ([1]), MDSDF ([2]), etc.
- | Phase-based data flow MoCCs : 6 DF MoCCs
  - Actors rate's pattern is cyclic
  - CSDF ([3]), FRDF ([4]), etc.
- | Data flow MoCCs with timing constraints : 2 DF MoCCs
  - Actors have a frequency and delay constraints
  - TPDF ([5]), PolyGraph ([6])

## Classification of data ow MoCCs II

- I Boolean-based data ow MoCCs : 3 DF MoCCs
  - DF MoCCs that have mechanism(s) triggered by boolean parameters
  - BDF ([7]), IDF ([8]), BPDF ([9])
- I Scenario-based data ow MoCCs : 4 DF MoCCs
  - DF MoCCs that have scenarios, i.e., actors' rates and/or execution time may vary
  - SADF ([10]), (P)FSM-SADF ([11], [12]), etc.
- I Data ow MoCC with Enable/Invoke capabilities : 5 DF MoCCs
  - DF MoCCs that endow actor with enable capability (i.e., asserts if an actor can re) and invoke capability (i.e., performs a re in that mode)
  - EIDF/CFDF ([13]), HCFDF ([14]), PSM-CFDF ([15])

# Classification of data ow MoCCs III

- | Data ow MoCC with unique features : 3 DF MoCCs
  - SPBDF ([16]): global state
  - HDF ([17]): combination of Finite State Machine and SDF
  - VRDF ([18]): parametric DF with many structural constraints
- | Process network-based data ow MoCCs : 2 DF MoCCs
  - Actors may have a state.
  - KPN ([19]), RPN ([20])
- | Meta-model for data ow MoCCs : 6 DF MoCCs
  - Additional rules on the top of a DF MoCC.
  - PSDF/PCSDF ([21]), HPDF ([22]), RDF ([23]), etc.

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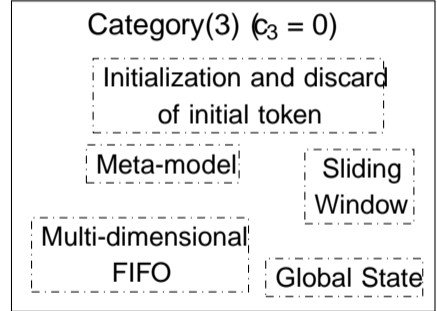
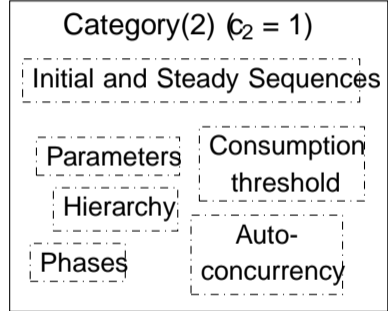
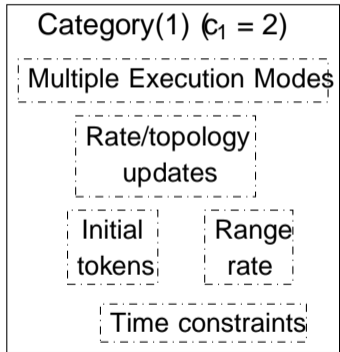
IV. Conclusion

# Expressiveness hierarchy: methodology

- 1 Characterize each DF MoCC according to well-defined features: rate/topology updates, range rate, parameters, etc.
- 2 Assign a score to feature and normalize it.
- 3 Assign a coefficient to each features' score.
- 4 Compute the expressiveness score by summing the normalized features' score with its coefficient.

# Expressiveness hierarchy: application

- Determining the best DF MoCC to model time-constrained and recon gurable CPS
- We classify feature from the best to the least important.



feature = score of feature

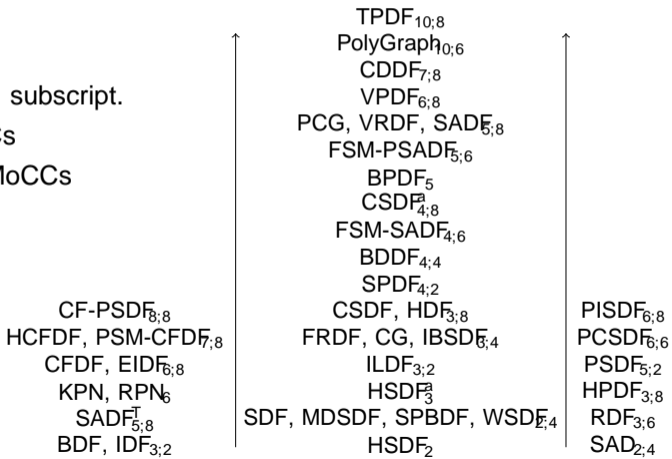
$c_i =$  expressiveness score

$$i \in \{1, 2, 3\} \Rightarrow \text{score} \in \text{category}(i)$$

# Expressiveness hierarchy: results

Expressiveness hierarchy of DF MoCCs well-suited to model time-constrained and recon gurable CPS.

- Expressiveness score shown as subscript.
- Left: Turing complete DF MoCCs
- Mid: Non-Turing complete DF MoCCs
- Right: Meta-model DF MoCCs



## Back to the ADAS

ADAS runs  
with finite memory  
(consistency)

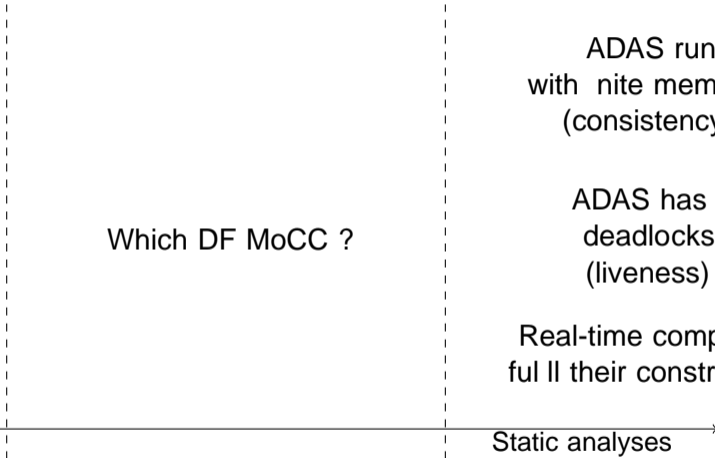
ADAS has no  
deadlocks  
(liveness)

Real-time components  
fulfill their constraints

Which DF MoCC ?

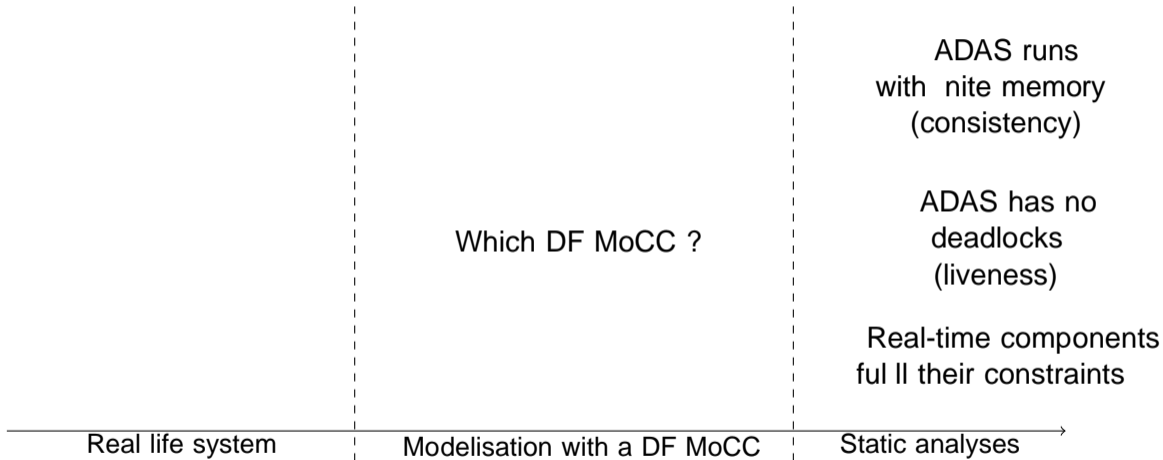
Real life system

Static analyses





# Back to the ADAS



Modelization of the ADAS with the DF MoCC PolyGraph.

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# Conclusion

- | A short survey on the main DF MoCCs for CPS design and verification.
  - Classification of DF MoCC in 9 categories.
  - Features and static analyses for a broad set of DF MoCCs.
- | A flexible expressiveness hierarchy.
  - Help designer's to choose the best DF MoCC for their needs.
  - Easily extensible.
  - Provide a reliable intuition rather than a strict claim.

# Conclusion

- | A short survey on the main DF MoCCs for CPS design and verification.
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Thank you for your attention. Feel free to ask any questions!



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