MCSoC 2025

18th IEEE INTERNATIONAL SYMPOSIUM ON EMBEDDED MULTICORE/MANY-CORE SYSTEMS-ON-CHIP (MCSoC-2025)

SINGAPORE | Dec. 15-18, 2025

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The 18th IEEE MCSoC 2025 will be held at **Newcastle Australia Institute of Higher Education – Singapore**

The Conference Presentation Rooms (Venue) are @ National Library Building of the Newcastle Australia Institute of Higher Education

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100 Victoria Street, #13-01/02 **National Library Building** Singapore 188064

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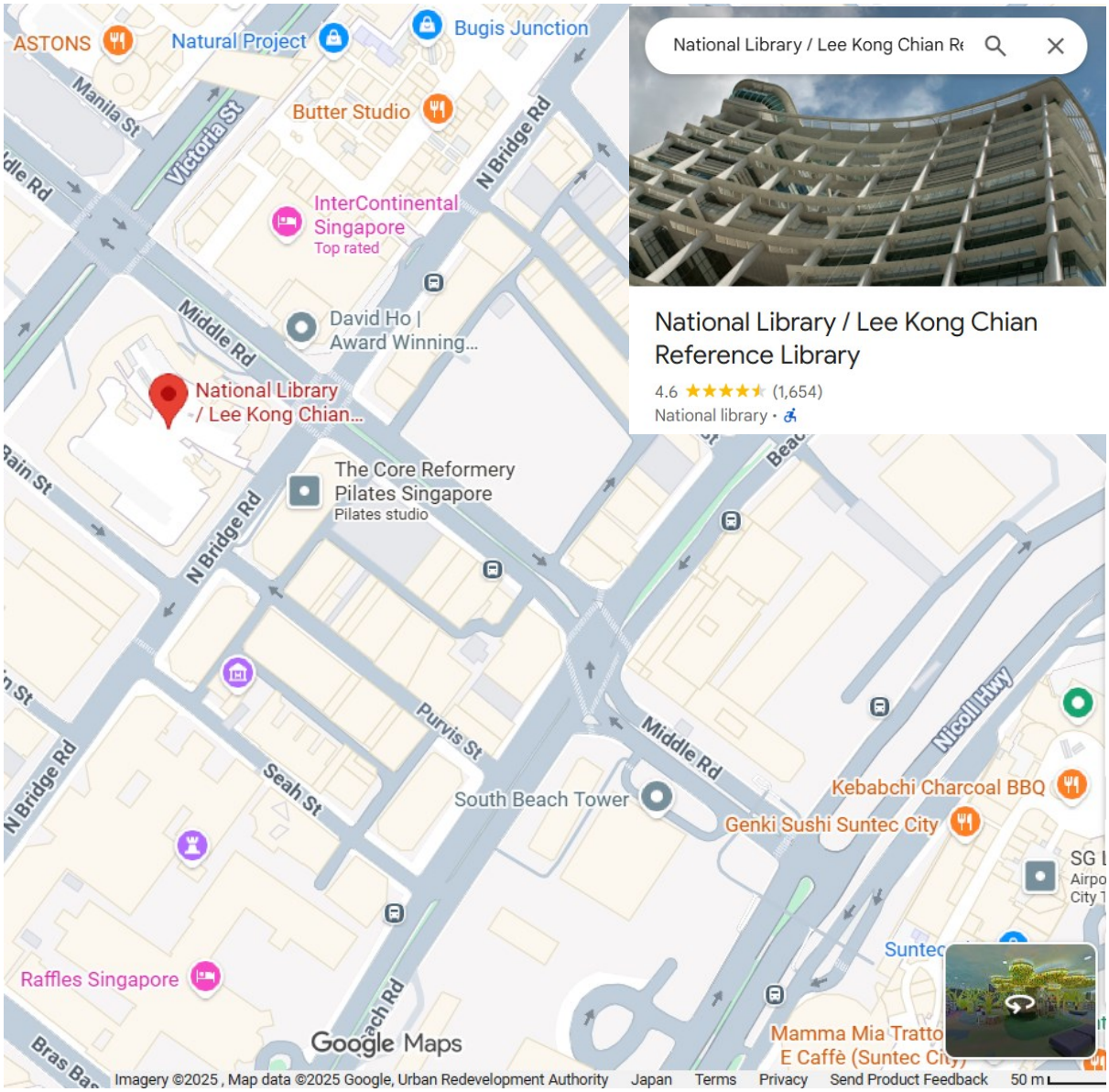


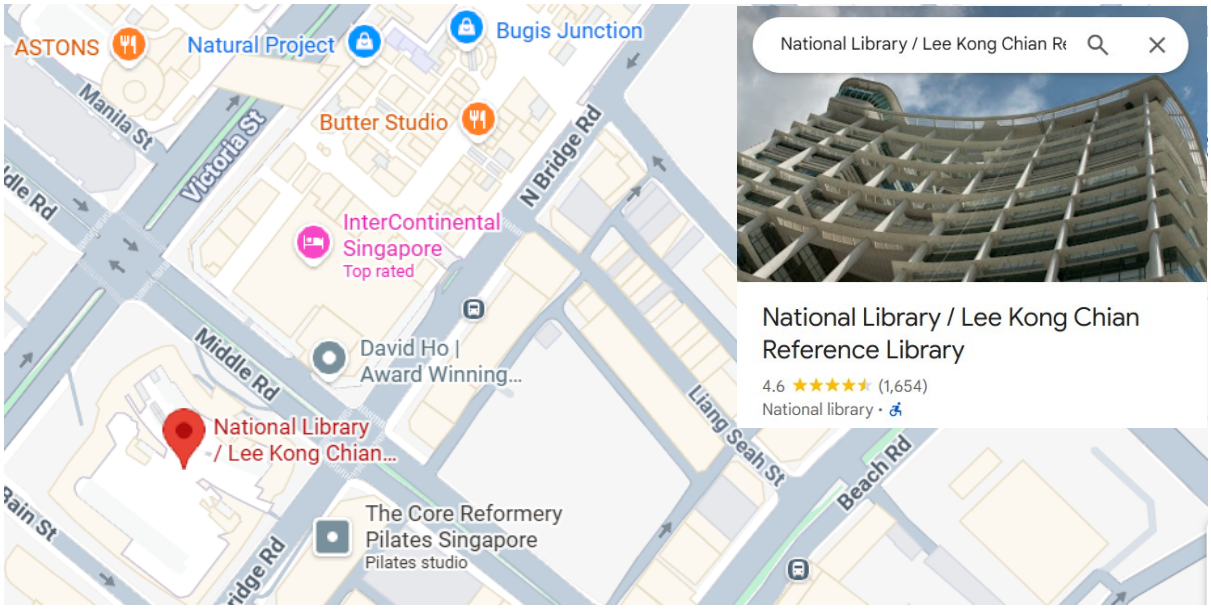
Join us for an unforgettable evening celebrating outstanding contributions in the field, with a formal dinner, networking, recognition of excellence, and a special **Honorary Keynote Address**.

Date: Wednesday | December 17, 2025 | 18:30 – 21:30

Eligibility: Included for full conference registrants

Additional tickets: $100.00

Address: National Library Building (NLB), 100 Victoria Street, #13-01, Singapore 188064 – **located at the conference venue**.



We look forward to celebrating achievements, hearing the Honorary Keynote, and sharing this special night with you!

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MCSoC 2025

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Mudar Sarem, *Manara University, Syria*
Xiaoming He, *Nanjing University of Posts and Telecommunications (NJUPT), China*
Guo-Wei Lu, *Kyushu University, Japan*
Mohamed Hamada, *The University of Aizu, Japan*
Chiang Liang Kok, *University of Newcastle, Australia*

Final Program for *18th IEEE International Symposium on Embedded Multicore/Manycore SoCs (MCSoC-2025)*

Time (Singapore)	Room A	Room B	Boardroom
Monday, December 15			
13:30-13:35	*Kickoff Session*		
13:35-14:35	**A1**: *Programming Techniques for Embedded Multicore/Manycore SoCs* Track 1 Chair(s): Chow Zi Jie (Singapore University of Technology and Design, Singapore & Chang Gung University, Taiwan), Michael Meyer (Eastern Washington University , U.S.A.) - RM	**B1**: *Performance Optimization and Auto-Tuning of Software on Multicore/Manycore Systems* S-Session 1 Chair(s): Masatoshi Kawai(Tohoku University, Japan), Qianrui Lin (SUTD, Singapore)	**WS1&2**: *Workshop* Workshop Session Chair: Kok Chiang Liang, University of Newcastle Australia, Singapore
14:35-15:35	**A2**: *Architectural Innovations in Embedded Multicore/Manycore SoCs* Track 2 Chair(s): Daisuke Suzuki (The University of Aizu, Japan), Archit Somani (Shiv Nadar Institution of Eminence, India)	**B2**: *Harnessing AI Tools for Transforming Education* S-Session 2 Chair(s): Teo Tee Hui (SUTD, Singapore), Muepu Mukendi Daniel (UoA, Japan)	**WS3**: *Workshop* Workshop Session Chair: Kok Chiang Liang, University of Newcastle Australia, Singapore
15:35-15:45	**CB1**: *Coffee/Tea Break*		
15:45-16:15	**B3**: *Cutting-Edge Developments in Immerging Applications I* S-Session 3 Chair(s): Mudar Sarem (Manara University, Syria), Deepika Saxena (The University of Aizu, Japan) -RM	**B4**: *Cutting-Edge Developments in Immerging Applications II* S-Session 4 Chairs: Khanh Dang (The University of Aizu, Japan), Bi Ye (Yongjiang Lab, China)	
16:15-17:15	**A3**: *Chiplet-Based Architectures and Design for Multicore SoCs* Track 3 Chair(s): Martin Radetzki (University of Stuttgart, Germany), Hanzhi Ma (Zhejiang University, China)	**B5**: *Machine Learning and Neuromorphic Computing for Edge and IoT II* S-Session 5 Chair(s): Wen Cheng Lai (Ming Chi University of Technology, Taiwan), Khanh Dang (The University of Aizu, Japan)	
17:15-18:00	**A4**: *Design Methodologies for Embedded Multicore/Manycore SoCs* Track 4 Chair(s): Teo Tee Hui (Singapore University of Technology and Design, Singapore)	**B6**: *Emerging Machine Learning and Deep Learning Models: Theory and Applications* S-Session 6 Chair(s): Haoli Zhao (Hebei University of Technology, China), Mridini Gawas (Goa University, India)	

Time (Singapore)	Room A	Room B	Boardroom
Tuesday, December 16			
09:00-09:20	**O2**: *Opening Session*		
09:20-10:20	**K1**: *Keynote 01: Intelligent & Perceptive Sensing and Actuation for Next-Generation Secure Chips - From Physical Design to Machine Learning (Massimo Alioto, Provost's Chair, Professor, National University of Singapore, Singapore)* Keynote Session Chair: Hideharu Amano, Professor Emeritus, Keio University and Senior Fellow, University of Tokyo, Japan		
10:20-10:30	**CB2**: *Coffee Break*		
10:30-11:30	**A5**: *Multicore SoCs for Cyber-Physical and Autonomous Systems* Track 5 Chair(s): Sebastian Haas (Barkhausen Institut, Germany), Trong-Thuc Hoang (The University of Electro-Communications, Japan)	**B7**: *Cutting-Edge Developments in Immerging Applications* S-Session Chair(s): Qianrui Lin (SUTD, Singapore), Kasem Khalil - RM) (University of Mississippi, U.S.A.)	
11:30-12:00	**D-Speaker 1**: *Neuromorphic Language Models (Jason K. Eshraghian, University of California, Santa Cruz, U.S.A)* Distinguished Speaker Session Chair(s): Fawaz Alazemi, Kuwait University, Kuwait	**D-Speaker 2**: *Rethinking AI at Mission-Critical Frontiers (Yoichi Tomioka, The University of Aizu, Japan)* Distinguished Speaker Session Chair: Teo Tee Hui, Singapore University of Technology and Design, Singapore	
12:00-13:30	*Lunch*		
13:30-14:30	**K2**: *Keynote 02: Agile-chip Platform: A Quick and Low-cost Chip Fabrication Approach for Edge Computing (Hideharu Amano, Professor Emeritus, Keio University and Senior Fellow, University of Tokyo, Japan)* Keynote Session Chair: Kiat Seng Yeo Singapore Univ. of Technology & Design, Singapore		
14:30-14:40	**CB3**: *Coffee Break*		
14:40-15:40	**A6**: *Interconnection Networks for Embedded Multicore/Manycore SoCs* Track 6 Chair(s): Wen Cheng Lai (Ming Chi University of Technology, Taiwan), Md Farhadur Reza (Eastern Illinois University, USA)	**B8**: *Embedded Neuromorphic Computing Systems* S-Session 8 Chair(s): Jason Eshraghian (UC Santa Cruz, USA), Tanja Harbaum (Karlsruhe Institute of Technology (KIT), Germany)	
15:50-16:50	**A7**: *Real-Time Systems for Embedded Multicore/Manycore SoCs*	**B9**: *Machine Learning and Neuromorphic Computing for Edge and IoT* S-Session 9 Chair(s): Yoon Seok	

Time (Singapore)	Room A	Room B	Boardroom
	Track 7 Chair(s): Kaijie Wei, Keio University, Japan	Yang (State Uni. of New York Korea, South Korea), Huakun Huang (Guangzhou Univ, China)	
17:00-18:00	**A8**: *Testing, Security, and Trust in Embedded Multicore/Manycore Systems* Track 8 Chair(s): Zheng Yue (The Chinese University of Hong Kong, Shenzhen, China), Sebastian Haas, Barkhausen Institut, Germany)	**B10**: *Embedded Applications and Ubiquitous Computing* S-Session 10 Chair(s): Zhishang Wang, The University of Aizu, Japan	
Wednesday, December 17			
09:00-10:00	**K3**: *Keynote 03: Malaysia's Chip Leap: Pioneering the Future of Semiconductors in Southeast Asia (Lee Hing Wah, Selangor Information Technology & Digital Economy Corporation (SIDEC), Malaysia))* Keynote Session Chair: Teo Tee Hui (Singapore University of Technology and Design, Singapore)		
10:00-10:10	*CB4: Coffee Break*		
10:10-11:10	**A9**: *Design Automation and Low-Power Techniques for Embedded Manycore SoCs* Track 9 Chair(s): Daisuke Suzuki , The University of Aizu, Japan	**B11**: *Embedded Machine Learning, and Data Analytics* S-Session 11 Chair(s): Takao Tomono, Keio University, Japan	
11:10-12:10	**A10**: *Sustainable Design and Lifecycle Management for Multicore SoCs* Track 10 Chair(s): Fawaz Alazemi, Kuwait University, Kuwait	**B12**: *Harnessing AI Tools for Transforming Education II* S-Session 12 Chair(s): Yiyang Fu, Singapore University of Technology and Design, Singapore	
12:10-13:40	*Lunch*		
14:00-15:00	**K4**: *Keynote 4: The Evolution of Processors: From CPUs to GPUs and Beyond (Won Woo Ro, Professor, School of Electrical and Electronic Engineering, Yonsei University, South Korea)* Session Chair: Khanh Dang, The University of Aizu, Japan		
15:00-15:10	*CB5: Coffee Break*		
15:10-16:10	**A11**: *Operating System Platforms for Real-Time Embedded Applications* Track 11 Chair(s): M Norazizi Sham Mohd Sayuti, Universiti Sains Islam Malaysia, Malaysia	**B13**: *Embedded, Cyber-Physical, and IoT Systems* S-Session 13 Chair(s): Yiqin Xiang (Zhejiang University, China & University of Illinois Urbana-Champaign,USA), Xinghang Tan (Zhejiang University, China)	

Time (Singapore)	Room A	Room B	Boardroom
16:10-17:10	**A12**: *Application Domains for Embedded Multicore/Manycore SoCs* Track 12 Chair(s): Sweta Kumari (Shiv Nadar Institute of Eminence, India), Kaijie Wei (Keio University, Japan)	**B14**: *Emerging Machine Learning and Deep Learning Models: Theory and Applications II* S-Session 14 Chair(s): Takao Tomono, Keio University, Japan	
17:15-18:15	**A13**: *Hardware Acceleration of AI on Embedded Edge SoCs* Track 13 Chair(s): Sean Longyu Ma, The University of Auckland, New Zeeland	**B15**: *Parallel/Distributed, Grid, and Cloud Computing* S-Session 15 Chair(s): Zhishang Wang (The University of Aizu, Japan), Mahadev Gawas (Directorate of Higher Education Goa,India)	
19:00-21:30	**K5-EHD**: *Conference Dinner, Evening Honorary Keynote & Best Paper Award Announcement* Navigating the VUCA World: Reflections on Research, Education, and the Future of Work (Kiat Seng Yeo Singapore University of Technology and Design (SUTD), Singapore)		
Thursday, December 18			
09:00-10:00	**A14**: *Hardware Acceleration of AI on Embedded Edge SoCs II* Track 14 Chair(s): Mark Deutel (Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany), Sean Longyu Ma (The University of Auckland, New Zeeland)	**B16**: *Emerging Machine Learning and Deep Learning Models: Theory and Applications* S-Session Chair(s): Mudar Sarem (Faculty of Engineering, Manara University, Latakia, Syria), Ali Bostani (American University of Kuwait, Kuwait)	
10:00-10:10	*CB6: Coffee Break*		
11:10-12:10	**A15**: *Machine Learning for Energy-Efficient and Reliable Manycore Systems* Track 15 Chair(s): Md Farhadur Reza, Eastern Illinois University, U.S.A.	**B17**: *Edge-AI and Resilient SoC Design for Autonomous and Secure Systems* S-Session 17 Chair(s): Mark Deutel, Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany	
12:10-12:15	**C**: *Closing session*		

Monday, December 15

Monday, December 15 13:30 - 13:35 (Asia/Singapore)

Kickoff Session

Room A, Room B, Boardroom

Monday, December 15 13:35 - 14:35 (Asia/Singapore)

A1: Programming Techniques for Embedded Multicore/Manycore SoCs

Track 1 Chair(s): Chow Zi Jie (Singapore University of Technology and Design, Singapore & Chang Gung University, Taiwan), Michael Meyer (Eastern Washington University , U.S.A.) - RM

Room A

As embedded systems evolve toward increasingly parallel and heterogeneous architectures, efficient programming techniques for multicore and manycore System-on-Chips (SoCs) have become critical. This session explores innovative software methodologies, compiler strategies, and runtime frameworks that address the challenges of scalability, performance, energy efficiency, and real-time responsiveness in embedded multicore environments. Presentations will cover a range of topics including parallel programming models, task scheduling, memory management, and domain-specific optimizations tailored for resource-constrained platforms. The session aims to bridge the gap between hardware capabilities and software productivity, fostering discussion on best practices and emerging paradigms in embedded parallel computing.

A1.1 13:35 ***Enhancing Static Task Scheduling for Pipelined Cyclic Executions on Heterogeneous Architectures***

Jonas Hollmann (Leibniz University Hanover, Germany); Jakob Arndt and Ioannis Kyriakopoulos (Infineon Technologies AG, Germany); Martin Friedrich (Leibniz Universität Hannover, Germany); Holger Blume (Leibniz Universitaet Hannover, Germany)

A1.2 13:50 ***Automating timing enclaves for reactive programs in Lingua Franca***

Julian Robledo and Jeronimo Castrillon (Technische Universität Dresden, Germany)

A1.3 14:05 ***HLS to FPGAs: extending software regions via transformations and offloading functions to the CPU***

Tiago Santos (University of Porto, Portugal & INESC TEC, Portugal); João Bispo (INESC TEC & University of Porto, Portugal); Joao M. P. Cardoso (University of Porto, Portugal); James C Hoe (Carnegie Mellon University, USA)

A1.4 14:20 ***A Policy-Driven Architecture for Verifiable Geo-Compliance in Programmable Networks***

Venkateswaran Dorai (Zscaler, USA)

Monday, December 15 13:35 - 14:35 (Asia/Singapore)

B1: Performance Optimization and Auto-Tuning of Software on Multicore/Manycore Systems

S-Session 1 Chair(s): Masatoshi Kawai(Tohoku University, Japan), Qianrui Lin (SUTD, Singapore)

Room B

As multicore and manycore architectures become increasingly complex and diverse, achieving optimal software performance requires more than conventional tuning. This session focuses on advanced techniques for performance optimization and auto-tuning across heterogeneous and parallel platforms. Topics include compiler-assisted tuning, adaptive runtime systems, workload-aware scheduling, and machine learning-based optimization strategies. Presenters will showcase methods that dynamically adjust software behavior to exploit architectural features, minimize bottlenecks, and maximize throughput and energy efficiency. The session aims to highlight scalable solutions that bridge the gap between theoretical performance and practical deployment in high-performance and embedded computing domains.

B1.1 13:35 ***Sparse Iterative Solvers Using High-Precision Arithmetic with Quasi Multi-Word Algorithms***

Daichi Mukunoki (Nagoya University, Japan); Katsuhisa Ozaki (Shibaura Institute of Technology, Japan)

B1.2 13:50 ***A Study on the Performance and Usability of Managed Memory and Unified Memory for Accelerating Numerical Calculation Program***

Satoshi Ohshima (Kyushu University, Japan); Akihiro Ida (Japan Agency for Marine-Earth Science and Technology, Japan); Masatoshi Kawai (Tohoku University, Japan); Takeshi Fukaya (Hokkaido University, Japan); Rio Yokota (Institute of Science Tokyo, Japan)

B1.3 14:05 ***A Review of FPGA-Driven LLM Acceleration***

Yulin Fu, Jiale Li, Cheng Cheng, Longyu Ma and Chiu Wing Sham (The University of Auckland, New Zealand); Nan Zou (Harbin Engineering University, China)

B1.4 14:20 ***Parallel Heuristic Semantic Walk on Large Knowledge Graphs with Text Embeddings***

Raj Singh Bisen, Vipul Kumar Chauhan, Parth Gupta, Sweta Kumari and Archit Somani (Shiv Nadar Institution of Eminence, India)

Monday, December 15 13:35 - 14:35 (Asia/Singapore)

WS1&2: Workshop

Workshop Session Chair: Kok Chiang Liang, University of Newcastle Australia, Singapore

''Digital Wellness Framework for Cybersecurity'' by V Sithira Vadivel and Peik Foong Yeap, University of Newcastle Australia, Australia

''Designing for Resiliency: A Physical Asset Management Perspective'', by Chee Kit Ho, C&W Services, U.S.A.

Room: Boardroom

Workshop 1 Abstract: Designed for educators, IT professionals, and organizational leaders, this workshop equips attendees with actionable strategies to integrate wellness principles into cybersecurity policies, training, and culture. The ultimate goal is to foster a digitally resilient community where security and well-being coexist, empowering individuals to thrive safely in an increasingly interconnected world.

Workshop 2 Abstract: Designed for engineers, facility managers, planners, and policymakers, this workshop provides practical insights into building resilient infrastructures that withstand environmental, technological, and economic challenges. By the end of the session, participants will be equipped with the tools and methodologies needed to transform traditional asset management into a proactive, resilience-driven discipline.

Monday, December 15 14:35 - 15:35 (Asia/Singapore)

A2: Architectural Innovations in Embedded Multicore/Manycore SoCs

Track 2 Chair(s): Daisuke Suzuki (The University of Aizu, Japan), Archit Somani (Shiv Nadar Institution of Eminence, India)

Room A

This session highlights cutting-edge architectural advancements that drive performance, scalability, and energy efficiency in embedded multicore and manycore System-on-Chips (SoCs). As applications demand higher computational throughput and tighter integration, researchers are exploring novel design paradigms-from heterogeneous cores and 3D integration to specialized accelerators and fault-tolerant mechanisms. Presentations in this session will showcase innovations in interconnects, memory hierarchies, power-aware architectures, and domain-specific customizations that push the boundaries of embedded computing. The session aims to foster dialogue on architectural strategies that enable next-generation intelligent systems across automotive, IoT, robotics, and edge AI domains.

A2.1 14:35 ***Data Allocation Rearrangement on CNN Accelerator based on Reshaping Systolic Tile Array using Planarized Matrix Reordering Techniques***

Hoseong Kim (Kyungpook National University, Korea (South)); Daejin Park (Kyungpook National University (KNU), Korea (South))

A2.2 14:50 ***FPGA-Based Highly Parallel Architecture for Multi-Robot Path Planning***

Kosei Nishio, Hasitha Waidyasooriya and Masanori Hariyama (Tohoku University, Japan)

A2.3 15:05 ***Exploring Spatial and Temporal Parallelism for Vision Transformer Acceleration***

Hasitha Waidyasooriya, Tomohiro Matsui, Daisuke Tanaka and Masanori Hariyama (Tohoku University, Japan)

A2.4 15:20 ***System and Method for Accelerating Multilinear Tensor Transformations using an Isomorphic Architecture and Efficient Sparse Processing***

Stanislav Sedukhin, Yoichi Tomioka and Kazuya Matsumoto (University of Aizu, Japan); Yuichi Okuyama (The University of Aizu, Japan)

Monday, December 15 14:35 - 15:35 (Asia/Singapore)

B2: Harnessing AI Tools for Transforming Education

S-Session 2 Chair(s): Teo Tee Hui (SUTD, Singapore), Muepu Mukendi Daniel (UoA, Japan)

Room B

Artificial Intelligence is reshaping the landscape of education, offering new possibilities for personalized learning, intelligent tutoring, curriculum design, and institutional management. This session explores how AI tools and frameworks are being leveraged to enhance teaching effectiveness, student engagement, and educational accessibility. Presentations will highlight innovations in adaptive learning systems, automated assessment, educational data analytics, and AI-driven content generation. By showcasing practical applications and research breakthroughs, the session aims to foster dialogue on the responsible and impactful integration of AI in classrooms, online platforms, and lifelong learning environments.

B2.1 14:35 ***PAMI-GPT: A Conversational Custom-GPT Model For Pattern Mining***

Madhavi Palla (University of Aizu, Japan); Arjun Chakravarthi Pogaku (The University of Aizu, Japan); Uday Kiran Kiran Rage (The University of Aizu, Japan & NICT, Japan)

B2.2 14:50 ***Towards Artificial Intelligence Chips Design: A Ground Up Approach for Beginners' Integrated Circuits Design Education***

Teo Tee Hui and Harsh Agarwal (Singapore University of Technology and Design, Singapore)

B2.3 15:05 ***Student Perspectives on AI-Powered Learning Tools: An Exploratory Study of DeepSeek, ChatGPT, and Gemini in Educational Settings***

Teo Tee Hui and Zi Jie Chow (Singapore University of Technology and Design, Singapore)

Monday, December 15 14:35 - 15:35 (Asia/Singapore)

WS3: Workshop

Workshop Session Chair: Kok Chiang Liang, University of Newcastle Australia, Singapore

''AI Applications for Worker Health & Safety and the Environment'' Charles Lee, University of Newcastle Australia, Australia

Room: Boardroom

Abstract: Participants will explore the intersection of AI and environmental management-leveraging intelligent systems to track emissions, reduce waste, and advance sustainable operations. Designed for engineers, safety officers, environmental managers, and policymakers, this workshop equips attendees with actionable strategies to harness AI for safer, healthier, and greener workplaces. The goal is to cultivate a forward-looking mindset where technology empowers resilience, accountability, and environmental stewardship.

Monday, December 15 15:35 - 15:45 (Asia/Singapore)

CB1: Coffee/Tea Break

Monday, December 15 15:45 - 16:15 (Asia/Singapore)

B3: Cutting-Edge Developments in Immerging Applications I

S-Session 3 Chair(s): Mudar Sarem (Manara University, Syria), Deepika Saxena (The University of Aizu, Japan) -RM

Room A

This session showcases pioneering research and transformative technologies driving the next wave of innovation across diverse application domains. From intelligent healthcare and autonomous systems to smart environments and edge AI, presenters will explore how multicore and manycore architectures are enabling breakthroughs in performance, adaptability, and real-world impact. Emphasis will be placed on novel use cases, cross-disciplinary integration, and system-level optimizations that push the boundaries of what embedded computing can achieve. The session invites discussion on how emerging applications are reshaping industries and inspiring new directions in system design and deployment.

B3.1 15:45 ***An Improved Deep Learning Based RGB-D Saliency Detection Model***

Mudar Sarem (Manara University, Syria); Zheng Yunping and Kejun Wang (South China University of Technology, China); Laya Albshlawy (Gen. Org of Remote Sensing, Syria)

B3.2 16:00 ***Bridging Cryptographic Robustness and Hardware Efficiency: A Comprehensive Analysis of S-Box Design Methodologies for SoC Integration***

Maitri Iyer (CSIR- CEERI Pilani, India); Jai Gopal Pandey (CSIR-Central Electronics Engineering Research Institute, Pilani, India)

Monday, December 15 15:45 - 16:15 (Asia/Singapore)

B4: Cutting-Edge Developments in Immerging Applications II

S-Session 4 Chairs: Khanh Dang (The University of Aizu, Japan), Bi Ye (Yongjiang Lab, China)

Room B

This session showcases pioneering research and transformative technologies driving the next wave of innovation across diverse application domains. From intelligent healthcare and autonomous systems to smart environments and edge AI, presenters will explore how multicore and manycore architectures are enabling breakthroughs in performance, adaptability, and real-world impact. Emphasis will be placed on novel use cases, cross-disciplinary integration, and system-level optimizations that push the boundaries of what embedded computing can achieve. The session invites discussion on how emerging applications are reshaping industries and inspiring new directions in system design and deployment.

B4.1 15:45 ***A Direct Spike Encoding for A Lightweight Neural Network Based ECG Classification***

Nanang Sulistiyanto, Raden Arief Setyawan and Made Wena Harilegawa

(Brawijaya University, Indonesia)

B4.2 16:00 ***An LLM-enabled Multi-Agent System for Evidence-Grounded Fact Checking***

Hong Ngoc Dao, Yasuhiro Hashimoto and Truong Cong Thang (The University of Aizu, Japan)

Monday, December 15 16:15 - 17:15 (Asia/Singapore)

A3: Chiplet-Based Architectures and Design for Multicore SoCs

Track 3 Chair(s): Martin Radetzki (University of Stuttgart, Germany), Hanzhi Ma (Zhejiang University, China)

Room A

As the demand for scalable, high-performance computing continues to grow, chiplet-based architectures are emerging as a transformative approach in multicore SoC design. This session explores the latest innovations in modular integration, inter-chiplet communication, packaging technologies, and design methodologies that enable flexible and efficient system construction. Presentations will highlight breakthroughs in heterogeneous chiplet composition, power and thermal management, and co-design strategies that address the challenges of yield, cost, and customization. By showcasing practical implementations and forward-looking research, the session aims to advance the dialogue on how chiplet-based systems are reshaping the future of multicore computing.

A3.1 16:15 ***Hybrid Interconnect and Intermediate Memory-Based 2.5D NoC Architecture for High Performance Computing Applications***

Lashmi Kondoth, Rajan Shankaran, Quan Z. Sheng and Endrowednes Kuantama (Macquarie University, Australia)

A3.2 16:30 ***Pipelined Scheduling and Communication Synthesis for Application-Specific Networks-on-Chip***

Martin Radetzki (University of Stuttgart, Germany)

A3.3 16:45 ***Instruction-Directed MAC for Efficient Classical Communication in Scalable Multi-Chip Quantum Systems***

Maurizio Palesi, Enrico Russo, Hamaad Rafique, Giuseppe Ascia and Davide Patti (University of Catania, Italy); Abhijit Das (Indian Institute of Technology Hyderabad, India); Sergi Abadal (Universitat Politècnica de Catalunya (UPC) & NaNoNetwoking Center in Catalunya (N3Cat), Spain)

A3.4 17:00 ***An Architectural Approach for the Secure Integration of Hardware Accelerators into a Trustworthy MPSoC Platform***

Sebastian Haas, Mattis Hasler, Friedrich Pauls and Christopher Dunkel (Barkhausen Institut, Germany); Yogesh Verma (Barkhausen Insitut, Germany); Nilanjana Das and Michael Raitza (Barkhausen Institut, Germany)

Monday, December 15 16:15 - 17:15 (Asia/Singapore)

B5: Machine Learning and Neuromorphic Computing for Edge and IoT II

S-Session 5 Chair(s): Wen Cheng Lai (Ming Chi University of Technology, Taiwan), Khanh Dang (The University of Aizu, Japan)

Room B, Boardroom

This session delves into the convergence of machine learning and neuromorphic computing to enable intelligent, low-power solutions for Edge and IoT applications. As systems become more distributed and resource-constrained, novel approaches are required to deliver real-time inference, adaptive behavior, and energy-efficient processing. Presentations will highlight advances in spiking neural networks, event-driven architectures, on-chip learning, and hardware-software co-design tailored for edge deployment. The session emphasizes scalable, biologically inspired models and their integration into practical IoT systems, fostering discussion on how neuromorphic paradigms and AI algorithms are transforming the future of embedded intelligence.

B5.1 16:15 ***GCNIM: A Booth-6T-SRAM based Graph-Convolutional-Networks-In-Memory Macro***

Yan Yan, Zhaoyang Zhang, Shaochen Li, Defa Wu, Jun Yang and Xin Si (Southeast University, China)

B5.2 16:30 ***IncineRate: Multi-Modal FPGA Accelerator Architecture for SCNNs***

Björn A Lindqvist (KTH Royal Institute of Technology, Sweden); Artur Podobas (KTH, Royal Institute of Technology, Sweden)

B5.3 16:45 ***CH2AI: Dynamic Checkpoint Scheduling of Anytime Neural Networks on Heterogeneous Units***

Matthias Stammler, Georgios Sotiropoulos, Julian Hoefer and Tanja Harbaum (Karlsruhe Institute of Technology, Germany); Krishnendu Guha (University College Cork, Ireland); Amlan Chakrabarti (Princeton University & University of Calcutta, USA); Juergen Becker (Karlsruhe Institute of Technology, Germany)

B5.4 17:00 ***Risk- and Quantization-aware Training for Convolutional Neural Networks***

Fumiaki Hayafuji and Yoichi Tomioka (University of Aizu, Japan); Yuichi Okuyama, Hiroshi Saito and Shogo Semba (The University of Aizu, Japan); Yuta Takahashi and Sumio Morioka (Interstellar Technologies Inc., Japan)

Monday, December 15 17:15 - 18:00 (Asia/Singapore)

A4: Design Methodologies for Embedded Multicore/Manycore SoCs

Track 4 Chair(s): Teo Tee Hui (Singapore University of Technology and Design, Singapore)

Room A

Designing efficient and scalable embedded multicore/manycore systems requires robust methodologies that address complexity, performance, and integration challenges. This session presents state-of-the-art approaches in system-level design, hardware/software co-design, modeling, simulation, and verification tailored for embedded platforms. Topics include design

automation, toolchains, power-aware optimization, and domain-specific frameworks that accelerate development cycles and enhance reliability. By showcasing practical techniques and emerging paradigms, the session aims to advance the design ecosystem for next-generation embedded computing across diverse application domains.

A4.1 17:15 ***Design and implementation of a high-performance RISC-V SoC for FPGAs with Linux support***

Yuki Yagi and Kenji Kise (Institute of Science Tokyo, Japan)

A4.2 17:30 ***Digital Dice Design using Pseudo Random Number Generator***

Teo Tee Hui (Singapore University of Technology and Design, Singapore); Maoyang Xiang (8 Somapah Rd & Singapore University Technology and Desgin, Singapore); Qianrui Lin and Michael Kee Han Lim (Singapore University of Technology and Design, Singapore)

A4.3 17:45 ***CFU Proving Ground: a hardware/software co-design framework for leveraging a custom function unit and RISC-V custom instructions***

Aoba Fujino (Institute of Science Tokyo, Japan); Kenji Kise (Tokyo Institute of Technology, Japan)

Monday, December 15 17:15 - 18:00 (Asia/Singapore)

B6: Emerging Machine Learning and Deep Learning Models: Theory and Applications

S-Session 6 Chair(s): Haoli Zhao (Hebei University of Technology, China), Mridini Gawas (Goa University, India)

Room B, Boardroom

This session explores the latest theoretical advancements and practical implementations in machine learning and deep learning, with a focus on emerging models that push the boundaries of intelligent computing. Presentations will cover novel architectures, training techniques, and optimization strategies that enhance model accuracy, efficiency, and generalization. Applications span diverse domains including computer vision, natural language processing, autonomous systems, and edge AI. By bridging foundational research with real-world deployment, the session aims to foster dialogue on scalable, robust, and interpretable learning systems for next-generation intelligent platforms.

B6.1 17:15 ***Heart Disease Monitoring System using AI Wireless Devices***

Dujdow Buranapanichkit, Apidet Booranawong, Nattha Jindapetch, Kiattisak Sengchuai and Susanna Saengsri (Prince of Songkla University, Thailand); Hiroshi Saito (The University of Aizu, Japan)

B6.2 17:30 ***An Approximate Dual Modular Redundancy Training Method for CNNs***

Kaho Kageyama, Yamato Saikawa and Yoichi Tomioka (University of Aizu, Japan); Hiroshi Saito (The University of Aizu, Japan)

B6.3 17:45 ***Autonomous Driving Model Training with 3D Gaussian Splatting Simulation and Limited Real-World Data***

Akira Sampei (University of Aizu, Japan); Yuichi Okuyama (The University of Aizu, Japan); Kensuke Kawana, Weiming Hu and Yoichi Tomioka (University of Aizu, Japan)

Tuesday, December 16

Tuesday, December 16 9:00 - 9:20 (Asia/Singapore)

O2: Opening Session

Tuesday, December 16 9:20 - 10:20 (Asia/Singapore)

K1: Keynote 01: Intelligent & Perceptive Sensing and Actuation for Next-Generation Secure Chips - From Physical Design to Machine Learning (Massimo Alioto, Provost's Chair, Professor, National University of Singapore, Singapore)

Keynote Session Chair: Hideharu Amano, Professor Emeritus, Keio University and Senior Fellow, University of Tokyo, Japan

Biography: Massimo Alioto is Provost's Chair Professor at the ECE Department of the National University of Singapore, where he leads the Green IC group, the Integrated Circuits and Embedded Systems area, and the FD-fAbrICS center on intelligent and connected systems. Previously, he held positions at the University of Siena, Intel Labs - CRL (2013), University of Michigan - Ann Arbor (2011-2012), University of California - Berkeley (2009-2011), and EPFL - Lausanne. He is (co)author of 400 publications in journals and conference proceedings, and four books with Springer (with two more coming). His primary research interests include ultra-low power and self-powered systems, green computing, circuits for machine intelligence, hardware security, and emerging technologies. He was the Editor in Chief of the IEEE Transactions on VLSI Systems and Deputy Editor in Chief of the IEEE Journal on Emerging and Selected Topics in Circuits and Systems. He was the Chair of the Distinguished Lecturer Program for the IEEE CAS Society and was a Distinguished Lecturer for the SSC and CAS Society. Previously, Prof. Alioto was the Chair of the "VLSI Systems and Applications" Technical Committee of the IEEE Circuits and Systems Society (2010-2012). He served as Guest Editor of numerous journal special issues (JSSC, TCAS-I, JETCAS...), Technical Program Chair of several IEEE conferences (ISCAS, SOCC, PRIME, ICECS), and TPC member (ISSCC, ASSCC). His research group's contribution has been recognized through various best paper awards (e.g., ISSCC), and in the ten technological highlights of the TSMC annual report. Prof. Alioto is an IEEE Fellow.

Abstract: Physical security of next-generation silicon systems mandates significant advances at their physical boundary, and hence in both on-chip sensing for attack detection and on-chip actuation for attack counteraction. This has recently motivated the investigation of a new breed of on-chip sensor interfaces and actuators that can continuously and inexpensively monitor the chip environment, gaining physical context awareness and capturing physical anomalies. This trend is increasingly converging with relentless advances in inexpensive on-chip (AI) intelligence, which can monitor physical signals and events to orchestrate the on-chip security ecosystem. In this keynote, the road towards ubiquitous intelligent & perceptive hardware security countermeasures is illustrated by analyzing recent silicon demonstrations with unprecedented capabilities to inexpensively perceive security events in real time and react to them intelligently (always-on). The new concept of hardware patching is also discussed, where circuit flexibility is introduced to make silicon chips able to evolve and counteract newly discovered vulnerabilities

through (machine) learning-based physical protection mechanisms.

Tuesday, December 16 10:20 - 10:30 (Asia/Singapore)

CB2: Coffee Break

Room A, Room B, Boardroom

Tuesday, December 16 10:30 - 11:30 (Asia/Singapore)

A5: Multicore SoCs for Cyber-Physical and Autonomous Systems

Track 5 Chair(s): Sebastian Haas (Barkhausen Institut, Germany), Trong-Thuc Hoang (The University of Electro-Communications, Japan)

Room A

Cyber-physical and autonomous systems demand high-performance, real-time, and energy-efficient computing platforms capable of interacting seamlessly with the physical world. This session focuses on the design, implementation, and optimization of multicore System-on-Chips (SoCs) tailored for such intelligent systems. Topics include real-time processing, sensor fusion, control algorithms, safety-critical architectures, and hardware/software co-design for robotics, automotive, aerospace, and industrial automation. Presentations will highlight innovations that enable reliable, low-latency, and adaptive behavior in dynamic environments, bridging the gap between embedded intelligence and physical autonomy.

10:30 ***Unifying IP Specification Through Formal Hardware Function Sets: An Industrial Case Study***

Robert Kunzelmann (Infineon Technologies AG, Germany & Technical University of Munich, Germany); Maximilian Berger (Infineon Technologies AG & Technical University of Munich, Germany); Vinod Bangalore Ganesh (Infineon Technologies AG & Technical University of Dresden, Germany); Rachana R Pai and Wolfgang Ecker (Infineon Technologies AG, Germany)

10:45 ***Low-Voltage 203dB High-Accuracy CMOS Exponential Function Generator***

Cosmin Radu Popa (UNSTPA, Romania & University Politehnica of Bucharest, Romania)

11:00 ***Improved Accuracy CMOS Sigmoidal Function Synthesizers***

Cosmin Radu Popa (UNSTPA, Romania & University Politehnica of Bucharest, Romania)

11:15 ***FlexSiMArch: An Extensible Simulator for Research and Development in Secure-by-Design Processor Technologies***

Sameer Mankotia and Daniel Conte de Leon (University of Idaho, USA)

Tuesday, December 16 10:30 - 11:30 (Asia/Singapore)

B7: Cutting-Edge Developments in Immerging Applications

S-Session Chair(s): Qianrui Lin (SUTD, Singapore), Kasem Khalil -RM) (University of Mississippi, U.S.A.)

Room B

This session presents forward-looking research and innovative solutions that harness multicore and manycore technologies to address the demands of rapidly evolving application domains. From intelligent mobility and digital health to smart infrastructure and immersive environments, presenters will explore how advanced system architectures and software frameworks are enabling new capabilities across sectors. Emphasis will be placed on cross-disciplinary integration, real-world deployment, and performance optimization tailored to emerging use cases. The session invites discussion on how these developments are shaping the future of embedded intelligence and transforming societal impact.

B7.1 10:30 ***A Study on Proactive Adaptation-Based Routing Strategies in 2D Network-on-Chip Architectures***

Lashmi Kondoth, Rajan Shankaran, Quan Z. Sheng and Endrowednes Kuantama (Macquarie University, Australia)

B7.2 10:45 ***Concurrent Multi-tasking using Metamorphic SW Replacement***

Janghun Lee (Kyungpook National University, Korea (South)); Daejin Park (Kyungpook National University (KNU), Korea (South))

B7.3 11:00 ***Secure and Intelligent Roaming Settlements Using Blockchain and AI***

Dinesh Kumar (Oracle America Inc, USA & University of Texas, Austin, USA); Ahmad Ahmad (Stock Plan Services, USA); Chandra P Jaiswal (NCAT, USA & Miracle Software System Inc., USA); Ravi Kumar (University of North Carolina at Charlotte, USA)

B7.4 11:15 ***Disaster Rescue Resource Allocation Based on the Ising Model***

Kosei Nakamoto, Masahito Kumagai, Masayuki Sato, Kazuhiko Komatsu and Hiroaki Kobayashi (Tohoku University, Japan)

Tuesday, December 16 11:30 - 12:00 (Asia/Singapore)

D-Speaker 1: Neuromorphic Language Models (Jason K. Eshraghian, University of California, Santa Cruz, U.S.A)

Distinguished Speaker Session Chair(s): Fawaz Alazemi, Kuwait University, Kuwait

Room A

Abstract: This talk shows the transformative potential of achieving sub-10-watt language models by drawing inspiration from the brain's energy efficiency. We demonstrate silicon results on Intel Loihi 2 in surpassing human-level throughput on billion-parameter models, setting a new benchmark for energy-efficient AI. This work not only redefined what's possible for low-power language models but also highlights the critical operations future accelerators must prioritize to enable the next wave of sustainable AI innovation.

Tuesday, December 16 11:30 - 12:00 (Asia/Singapore)

D-Speaker 2: Rethinking AI at Mission-Critical Frontiers (Yoichi

Tomioka, The University of Aizu, Japan)

Distinguished Speaker Session Chair: Teo Tee Hui, Singapore University of Technology and Design, Singapore

Room B, Boardroom

Tuesday, December 16 12:00 - 13:30 (Asia/Singapore)

Lunch

Room A, Room B

Tuesday, December 16 13:30 - 14:30 (Asia/Singapore)

K2: Keynote 02: Agile-chip Platform: A Quick and Low-cost Chip Fabrication Approach for Edge Computing (Hideharu Amano, Professor Emeritus, Keio University and Senior Fellow, University of Tokyo, Japan)

Keynote Session Chair: Kiat Seng Yeo Singapore Univ. of Technology & Design, Singapore

Biography: Hideharu Amano earned his Ph.D. in Electrical Engineering from the Graduate School of Keio University in 1986. Currently, he serves as a senior fellow at the System Design Laboratory in the Graduate School of Engineering at the University of Tokyo. Additionally, he is a Professor Emeritus at Keio University and is affiliated with the Agile-X Project at the University of Tokyo.

Abstract: The Agile-X (Agile-chip) platform is a type of Structured ASIC that enables the creation of LSI in a short period and at a low cost. In this method, only the wiring between gate arrays on a base chip, manufactured like a conventional ASIC using lower-layer wiring, is produced using Minimal-Fab. This allows any circuit to be manufactured based on the designer's specified GDS file. The performance evaluation of the Agile-chip platform compared to FPGAs and experiences of using semiconductor education are introduced.

Tuesday, December 16 14:30 - 14:40 (Asia/Singapore)

CB3: Coffee Break

Room A, Room B, Boardroom

Tuesday, December 16 14:40 - 15:40 (Asia/Singapore)

A6: Interconnection Networks for Embedded Multicore/Manycore SoCs

Track 6 Chair(s): Wen Cheng Lai (Ming Chi University of Technology, Taiwan), Md Farhadur Reza (Eastern Illinois University, USA)

Room A

Efficient interconnection networks are the backbone of scalable multicore and manycore System-on-Chip (SoC) architectures. This session focuses on the design, analysis, and optimization of on-chip communication infrastructures that enable high-throughput, low-latency, and energy-aware data exchange among processing elements. Topics include Network-on-Chip (NoC) topologies, routing algorithms, congestion control, fault tolerance, and emerging

technologies such as 3D integration and silicon photonics. Presentations will highlight innovations that address the growing complexity of embedded systems, ensuring reliable and adaptive communication for next-generation applications in AI, IoT, and cyber-physical systems.

A6.1 14:40 ***Routing in Multi-Chip Platforms with Hybrid Interconnects***

Joy Halder (Postdoctoral Researcher, Technical University Dresden, Germany); Nayeem Ahmed and Viktor Razilov (Technische Universität Dresden, Germany); Emil Matus (TU Dresden, Germany); Gerhard P. Fettweis (Technische Universität Dresden, Germany)

A6.2 14:55 ***Toward Predictable Deflection Routing in Routerless NoCs for Real-Time Systems***

M Norazizi Sham Mohd Sayuti (Universiti Sains Islam Malaysia, Malaysia); Leandro Soares Indrusiak (University of Leeds, United Kingdom (Great Britain))

A6.3 15:10 ***Power and Performance Evaluation of Spidergon and Mesh Topology in Network-on-Chip***

Sai Kumar Reddy (MNIT Jaipur, India); Mushtaq Ahmed (Malaviya National Institute of Technology Jaipur INDIA, India); Agam Kumar Singh (MNIT Jaipur, India); Bhavna Ambudkar (Symbiosis Institute of Technology, India & Symbiosis International University, India)

A6.4 15:25 ***Reliable loop set for Routerless Network-on-chip***

Fawaz Alazemi and Zaid Hussain (Kuwait University, Kuwait); Bader F AlBdaiwi (Kuwait University, Luxembourg)

Tuesday, December 16 14:40 - 15:40 (Asia/Singapore)

B8: Embedded Neuromorphic Computing Systems

S-Session 8 Chair(s): Jason Eshraghian (UC Santa Cruz, USA), Tanja Harbaum (Karlsruhe Institute of Technology (KIT), Germany)

Room B

Neuromorphic computing offers a paradigm shift in how embedded systems process information-mimicking the brain's architecture to achieve energy-efficient, event-driven, and adaptive computation. This session explores the design and deployment of embedded neuromorphic systems, focusing on spiking neural networks, specialized hardware accelerators, and sensor-integrated platforms. Presentations will highlight innovations in low-power learning, real-time inference, and biologically inspired architectures tailored for edge AI, robotics, and IoT applications. By bridging neuroscience principles with embedded engineering, the session aims to advance the development of intelligent systems that operate efficiently in dynamic, resource-constrained environments.

B8.1 14:40 ***Evolutionary Algorithm for STDP-based Spiking Neural Network Model Compression***

Yuga Hanyu, Zhishang Wang and Khanh N. Dang (University of Aizu, Japan)

B8.2 14:55 ***MindCore: Spike-Driven Programmable Accelerator for On-device***

Neuromorphic Computing

Hawon Park, Si Yong Lee, Ryangjin Lee and Yoora Kim (Stony Brook University, USA); Yoon Seok Yang (SUNY Korea University, Korea (South))

B8.3 15:10 ***Vision spiking Transformer for Image Classification***

Yiqin Xiang (Zhejiang University, China & University of Illinois Urbana-Champaign, USA); Teo Tee Hui (Singapore University of Technology and Design, Singapore); Junwen Zhang and Hanzhi Ma (Zhejiang University, China)

B8.4 15:25 ***Embedded FPGA Acceleration of Brain-Like Neural Networks: Online Learning to Scalable Inference***

Muhammad Ihsan Al Hafiz and Naresh Ravichandran (KTH Royal Institute of Technology, Sweden); Anders Lansner (KTH Royal Institute of Technology and Stockholm University, Sweden); Pawel Herman and Artur Podobas (KTH Royal Institute of Technology, Sweden)

Tuesday, December 16 15:50 - 16:50 (Asia/Singapore)

A7: Real-Time Systems for Embedded Multicore/Manycore SoCs

Track 7 Chair(s): Kaijie Wei, Keio University, Japan

Room A

Real-time systems are at the heart of safety-critical and latency-sensitive applications, where deterministic behavior and timely execution are paramount. This session focuses on the design, analysis, and implementation of real-time solutions for embedded multicore and manycore System-on-Chips (SoCs). Topics include scheduling algorithms, timing analysis, resource management, and hardware/software co-design techniques that ensure predictability and responsiveness under stringent constraints. Presentations will highlight innovations in real-time operating systems, mixed-criticality systems, and verification frameworks tailored for domains such as automotive, aerospace, robotics, and industrial automation. The session aims to advance the state of the art in dependable and high-performance real-time embedded computing.

A7.1 15:50 ***A Comprehensive Study on Execution Right Delegation Scheduling Algorithm for Multiprocessors***

Takaharu Suzuki and Kiyofumi Tanaka (Japan Advanced Institute of Science and Technology, Japan)

A7.2 16:05 ***Reducing Transmission Overhead in Edge-Assisted Visual SLAM: Compact Serialization and State-Adaptive Transmission***

Chenzhang Xia (Kyushu University, Japan); Koji Inoue (Kyushu University Japan, Japan)

A7.3 16:20 ***FPGA-based Muon Beam Monitoring with Real-Time Fault Recovery***

Yoshiki Yamada (University of Tsukuba, Japan); Yoshiki Yamaguchi (University of Tsukuba, Japan & Kumamoto University, Japan); Kenya Okabe (The Graduate University for Advanced Studies, Japan); Yowichi Fujita, Yoshinori Fukao, Eitaro Hamada, Youichi Igarashi, Masayoshi Shoji and Hironori Uchinoyae (High Energy Accelerator Research Organization, Japan); Tetsuichi Kishishita (University of Bonn,

Germany); Kazuki Ueno (The University of Osaka, Japan)

A7.4 16:35 ***Response Time Analysis of CIL-EDF Scheduling for ROS2 Multi-threaded Executors***

Zhengda Wu (Sun Yat-sen University, China & Academy of Military Science, China); Ruihao Chen (China Academy of Launch Vehicle Technology, China); Yixiao Feng (National Innovation Institute of Defense Technology, China); mingtai lv (Acadamy of Military Science, China); Sining Yang (Intelligent Gaming and Decision-Making Laboratory, China); Lulu Wang (Artificial Intelligence Research Center, National Innovation Institute of Defense Technology, China); Hanyan Huang (Sun Yat-sen University, China)

Tuesday, December 16 15:50 - 16:50 (Asia/Singapore)

B9: Machine Learning and Neuromorphic Computing for Edge and IoT

S-Session 9 Chair(s): Yoon Seok Yang (State Uni. of New York Korea, South Korea), Huakun Huang (Guangzhou Univ, China)

Room B

Edge and IoT systems are increasingly expected to perform intelligent tasks with minimal latency and power consumption. This session explores the convergence of machine learning and neuromorphic computing as a pathway to meet these demands. Presentations will highlight innovations in lightweight inference models, spiking neural networks, event-driven processing, and hardware-software co-design tailored for edge deployment. Emphasis will be placed on real-time adaptability, energy efficiency, and biologically inspired architectures that enable smart sensing, decision-making, and autonomous behavior in distributed environments. The session aims to advance the dialogue on scalable, low-power intelligence for next-generation embedded systems.

B9.1 15:50 ***Profiling Data Movement in SNN Memory Hierarchies***

Isaac Chee (University of California, Santa Cruz, USA); Subrahamanian Hari, Kaustubh Harnoor, Colleen Josephson and Jason Eshraghian (University of California Santa Cruz, USA)

B9.2 16:05 ***Early-Exit Neural Architecture Search for Energy-Harvesting Edge Computing***

Pierre-Louis Sixdenier (Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany); Mark Deutel (Friedrich-Alexander-Universität Erlangen-Nürnberg & Fraunhofer Institute for Integrated Circuites IIS, Germany); Jürgen Teich (Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany)

B9.3 16:20 ***DNN-based Optimal Partial Offloading in Multi-User Multi-Server MEC Networks***

Hoa Tran-Dang (Kumoh National Institute of Technology, Korea (South) & IT Convergence Engineering, Korea (South)); Dong Seong Kim (Kumoh National Institute of Technology, Korea (South))

B9.4 16:35 ***FSPC: A Lossy Spike Compression Through Correlated-AER Merging In***

Spiking Neural Networks

Satvik Ganesh, Yuga Hanyu, Zhishang Wang and Khanh N. Dang (University of Aizu, Japan)

Tuesday, December 16 17:00 - 18:00 (Asia/Singapore)

A8: Testing, Security, and Trust in Embedded Multicore/Manycore Systems

Track 8 Chair(s): Zheng Yue (The Chinese University of Hong Kong, Shenzhen, China), Sebastian Haas, Barkhausen Institut, Germany)

Room A

As embedded multicore and manycore systems become integral to critical infrastructure and intelligent applications, ensuring their reliability, security, and trustworthiness is paramount. This session focuses on rigorous testing methodologies, hardware and software security mechanisms, and trust models tailored for complex, parallel architectures. Topics include fault detection and tolerance, secure boot and runtime environments, side-channel attack mitigation, and formal verification techniques. Presentations will highlight innovations that safeguard system integrity across domains such as automotive, aerospace, healthcare, and industrial automation. The session aims to foster resilient design practices and trustworthy deployment strategies for next-generation embedded platforms.

A8.1 17:00 ***A Co-design of Lossy Compression and Error Correction for Approximate Communication***

Yao Hu (The University of Tokyo, Japan)

A8.2 17:15 ***A Machine Learning-Based Decision Aid for Predictive Maintenance Using Fault Diagnosis Data***

Said Almaqbali (MMU, Malaysia); Asmaa H. Marhoubi (University of Technology and Applied Sciences, Oman); Oualid Ben Ali (Applied Science University, Manama, Kingdom of Bahrain, Bahrain)

A8.3 17:30 ***Secure Multimodal Data Encryption using CRT-Based Encryption and MITM-Resilient Hybrid ElGamal-AES***

Ravinder Singh (Malaviya National Institute of Technology Jaipur, India); Agam Kumar Singh (MNIT Jaipur, India); Mushtaq Ahmed (Malaviya National Institute of Technology Jaipur INDIA, India)

Tuesday, December 16 17:00 - 18:00 (Asia/Singapore)

B10: Embedded Applications and Ubiquitous Computing

S-Session 10 Chair(s): Zhishang Wang, The University of Aizu, Japan

Room B

As computing becomes increasingly pervasive, embedded systems are playing a central role in enabling seamless, intelligent interactions across everyday environments. This session explores innovative applications and system-level solutions that harness multicore and manycore technologies to support ubiquitous computing. Topics include context-aware systems, wearable

and ambient intelligence, smart environments, and real-time data processing at the edge. Presentations will highlight how embedded platforms are being integrated into diverse domains-from healthcare and mobility to industrial automation and consumer electronics-pushing the boundaries of connectivity, adaptability, and user-centric design.

B10.1 17:00 ***Cost-Effective Kubernetes at the Edge: A Comparative Analysis of K3s on Raspberry Pi versus Cloud Deployments***

Srivenkateswara Reddy Sankiti (Cleveland State University, USA); Vinoth Punniyamoorthy (JPMorgan Chase, USA); Shiva Kumar Reddy Carimireddy (Fidelity Investments, USA); Ashok Gadi Parthi (Verizon, USA); Nachiappan Chockalingam (Meta, USA); Kabilan Kannan (AMD, USA); Suhas Malempati (The Cato Corporation, USA); Akash K Agarwal (Albertsons Companies Inc, USA)

B10.2 17:15 ***Infrastructure Design of Vehicular ad Hoc Network with Algorithm***

Wen Cheng Lai (National Taiwan University of Science and Technology, Taiwan)

B10.3 17:30 ***Advancing Intelligent Surveillance: Immediate Identification of Violence and Theft Utilizing YOLOv11 and SlowFast Networks***

Khoi Pham Dang, Huy Gia Huu Ngo and Trung Nguyen Quoc (FPT University, Vietnam); Kiet Tran-Trung and Vinh Truong Hoang (Ho Chi Minh City Open University, Vietnam)

Wednesday, December 17

Wednesday, December 17 9:00 - 10:00 (Asia/Singapore)

K3: Keynote 03: Malaysia's Chip Leap: Pioneering the Future of Semiconductors in Southeast Asia (Lee Hing Wah, Selangor Information Technology & Digital Economy Corporation (SIDEC), Malaysia))

Keynote Session Chair: Teo Tee Hui (Singapore University of Technology and Design, Singapore)

Biography: Dr. Lee Hing Wah graduated with a PhD in Mechanical Engineering (MEMS) from the University of Science Malaysia (USM) and has more than 19 years of industrial experience as a researcher, professional technologist, policy maker, international standards committee member, and semiconductor ecosystem builder. Currently leading the Semiconductor & Venture Division in Sidec, which manages the Malaysia Semiconductor IC Design Park. His responsibilities include driving the strategic vision and execution of Malaysia's flagship initiative to become a global hub for semiconductor and integrated circuit (IC) design. This role sits at the intersection of technology foresight, ecosystem building, talent development, and international engagement, in support of the National Semiconductor Strategy (NSS) and Malaysia Silicon Vision. His research and technology development experience includes semiconductor technologies such as IC design, advanced packaging, WBGSs, other niche areas such as AI devices, HBM, photonics, memristors, etc.; nanomaterials and 2D-NM synthesis and characterization (ferromagnetic nanoparticles, metal oxide nanowires, carbon nanotubes, graphene and their derivatives); incorporation of nanomaterials on MEMS and NEMS device platforms for sensor and electronics applications; printed, flexible, and wearable electronics. He has 50 filed patents and journal publications.

Abstract: As Southeast Asia rises to prominence in the global semiconductor industry, Malaysia stands at the forefront with its groundbreaking initiative, the Malaysia Semiconductor IC Design Park. This keynote session, delivered by Yong Kai Ping, CEO of SIDEC, will explore the strategic vision behind this transformative project, its role in positioning Malaysia as a regional leader, and its impact on the global semiconductor landscape. The session will delve into how the IC Design Park, supported by the collaboration of federal and state governments, global technology firms, and venture capitalists, is creating an ecosystem that fosters innovation, talent development, and sustainable growth. The park is designed to attract cutting-edge IC design companies, offering advanced infrastructure, Electronic Design Automation (EDA) tools, and critical industry partnerships. Yong Kai Ping will highlight key milestones of the initiative, including the role of the Malaysia Advanced Semiconductor and AI Academy in training the next generation of engineers, and the establishment of the RM100 million Semiconductor Venture Fund, which aims to fuel the growth of high-potential semiconductor companies in Malaysia. Join this keynote to gain insight into how Malaysia is pioneering the future of semiconductors in Southeast Asia and laying the groundwork for a new era of technological leadership in the region.

Wednesday, December 17 10:00 - 10:10 (Asia/Singapore)

CB4: Coffee Break

Room A, Room B, Boardroom

Wednesday, December 17 10:10 - 11:10 (Asia/Singapore)

A9: Design Automation and Low-Power Techniques for Embedded Manycore SoCs

Track 9 Chair(s): Daisuke Suzuki , The University of Aizu, Japan

Room A

As embedded manycore systems scale in complexity and application diversity, efficient design automation and power optimization have become critical enablers of performance and sustainability. This session focuses on methodologies and tools that streamline the design process while minimizing energy consumption across compute-intensive and resource-constrained environments. Topics include high-level synthesis, power-aware design flows, dynamic voltage and frequency scaling (DVFS), clock gating, and machine learning-assisted optimization. Presentations will highlight innovations that reduce design time, enhance reliability, and extend battery life-paving the way for energy-efficient, high-performance embedded systems in edge AI, IoT, and mobile computing.

A9.1 10:10 ***Cross-layer Approximate Computing and Critical Path Isolation for Energy-Efficient and Variation-Tolerant Design***

Meisei Yamaguchi, Yutaka Masuda and Tohru Ishihara (Nagoya University, Japan)

A9.2 10:25 ***Utilizing Wide Range Energy/Delay Tradeoffs in Logarithmic Multipliers to Reduce Energy Dissipated for AI Inference Workloads***

Tai-Feng Chen, Yutaka Masuda and Tohru Ishihara (Nagoya University, Japan)

A9.3 10:40 ***Real-time In-sensor Computing: An 8-bit ADC-less CMOS sensing for Image edge detection***

Adway Paul, Samanway Pal and Nirmoy Modak (Jadavpur University, India)

A9.4 10:55 ***A High Level Synthesis Tool for Multiple FPGAs***

Kazutoshi Wakabayashi (The Universtiy of Tokyo, Japan); Wataru Takahashi (NEC, Japan); Hideharu Amano (Keio University, Japan)

Wednesday, December 17 10:10 - 11:10 (Asia/Singapore)

B11: Embedded Machine Learning, and Data Analytics

S-Session 11 Chair(s): Takao Tomono, Keio University, Japan

Room B

As intelligent systems increasingly operate at the edge, embedding machine learning and data analytics capabilities directly into resource-constrained platforms has become essential. This session explores the integration of learning algorithms and analytical frameworks within embedded multicore and manycore architectures. Topics include lightweight inference models, real-time data processing, feature extraction, and hardware-software co-optimization for edge AI and IoT applications. Presentations will highlight innovations that enable adaptive, low-latency decision-making and efficient data utilization across domains such as smart healthcare, autonomous systems, and industrial monitoring. The session aims to advance the frontier of embedded intelligence through scalable and context-aware analytics.

B11.1 10:10 ***Unsupervised Learning of Variational Autoencoders on Cortex-M Microcontrollers***

Mark Deutel (Friedrich-Alexander-Universität Erlangen-Nürnberg & Fraunhofer Institute for Integrated Circuites IIS, Germany); Axel Plinge (Fraunhofer IIS, Germany); Dominik Seuß (Fraunhofer Institute for Integrated Circuits IIS, Germany); Christopher Mutschler (Fraunhofer IIS, Germany); Frank Hannig and Jürgen Teich (Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany)

B11.2 10:25 ***Adaptive Retrieval-Augmented Generative Intelligent Tutoring System for Automata Theory***

Youssef Yuto Obata (University of Aizu, Japan); Mohamed Hamada (UoA, Japan)

B11.3 10:40 ***Predictive Modeling of Submissions and Learning Outcomes in Online Judge Systems***

Md. Shahajada Mia (The University of Aizu, Japan); Yutaka Watanobe (University of Aizu, Japan); Md. Mostafizer Rahman (Tulane University, USA); Md Faizul Ibne Amin and Daniel Muepu Mukendi (The University of Aizu, Japan)

B11.4 10:55 ***Performance Optimization of Machine Inference Applications on Edge Devices with a RISC-V Custom Instruction***

Daichi Higashi and Hitoshi Oi (The University of Aizu, Japan)

Wednesday, December 17 11:10 - 12:10 (Asia/Singapore)

A10: Sustainable Design and Lifecycle Management for Multicore SoCs

Track 10 Chair(s): Fawaz Alazemi, Kuwait University, Kuwait

Room A

As environmental and economic pressures intensify, sustainability has become a central concern in the design and deployment of multicore System-on-Chips (SoCs). This session explores methodologies and technologies that promote energy efficiency, resource-aware design, and long-term reliability across the entire lifecycle of embedded systems. Topics include eco-conscious design automation, thermal and power management, aging-aware architectures, and strategies for recyclability and end-of-life optimization. Presentations will highlight innovations that balance performance with sustainability, enabling multicore SoCs to meet the demands of modern applications while minimizing ecological impact. The session aims to foster dialogue on responsible engineering practices for future-ready computing platforms.

11:10 ***FP-FBEMS: FPGA-based Optimization of Forward/Backward EMS Decoding for CV-QKD***

Kaijie Wei (Keio University, Japan); Devanshu Garg (Blueqat Inc., Japan); Ryutaro Nagai (SCSK Corporation, Japan); Takao Tomono (Keio University, Japan); Hideharu Amano (The University of Tokyo, Japan)

11:30 ***History-Correlated Stride Bank Prediction for Tightly Coupled Memory Systems***

Ipek Gecin, Emil Matus and Gerhard P. Fettweis (Vodafone Chair Mobile Communications Systems, TU Dresden, Germany)

11:50 ***Polarization Ray Tracing for Multi-Axis Optical Systems in Non-Sequential Mode***

Ye Bi (Yongjiang Laboratory, China); Shujin Zheng, Tianwen Hou, Yi Jiang, Shengnan Qin and Chengrui Le (Advanced Display and Sensing Research Center, China)

Wednesday, December 17 11:10 - 12:10 (Asia/Singapore)

B12: Harnessing AI Tools for Transforming Education II

S-Session 12 Chair(s): Yiyang Fu, Singapore University of Technology and Design, Singapore

Room B

Artificial Intelligence is reshaping the educational landscape by enabling personalized learning, intelligent tutoring, and data-driven decision-making. This session explores the integration of AI tools into educational systems, focusing on scalable platforms, adaptive content delivery, and real-time analytics that enhance teaching and learning outcomes. Presentations will highlight innovations in curriculum design, assessment automation, and inclusive learning environments powered by machine learning, natural language processing, and multimodal interfaces. By bridging pedagogy with technology, the session aims to foster transformative strategies that empower educators and learners in diverse contexts.

B12.1 11:10 ***A Quantitative Framework for Layer-Wise Material Selection in MOSFETs Using Priority-Aware Property Mapping***

Teo Tee Hui, Yiyang Fu, Fage Liu, Zhengyao He and Qianrui Lin (Singapore University of Technology and Design, Singapore)

B12.2 11:25 ***Performance Comparison for CPU, FPGA, and GPU in CRS Format Conversion Processing***

Tomoya Yokono and Keisuke Sugiura (University of Tsukuba, Japan); Yoshiki Yamaguchi (University of Tsukuba, Japan & Kumamoto University, Japan)

B12.3 11:40 ***Comparative Evaluation of ChatGPT, Gemini, and DeepSeek in Educational Problem Solving***

Daniel Muepu Mukendi (The University of Aizu, Japan); Yutaka Watanobe (University of Aizu, Japan); Md Faizul Ibne Amin and Md. Shahajada Mia (The University of Aizu, Japan)

B12.4 11:55 ***Bridging the Plausibility-Validity Gap by Fine-Tuning a Reasoning-Enhanced LLM for Chemical Synthesis and Discovery***

Malikussaid, Hilal H. Nuha and Isman Kurniawan (Telkom University, Indonesia)

Wednesday, December 17 12:10 - 13:40 (Asia/Singapore)

Lunch

Wednesday, December 17 14:00 - 15:00 (Asia/Singapore)

K4: Keynote 4: The Evolution of Processors: From CPUs to GPUs and Beyond (Won Woo Ro, Professor, School of Electrical and Electronic Engineering, Yonsei University, South Korea)

Session Chair: Khanh Dang, The University of Aizu, Japan

*

Biography: Won Woo Ro received the B.S. degree in Electrical Engineering from Yonsei University, Seoul, South Korea, in 1996, and the M.S. and Ph.D. in Electrical Engineering from the University of Southern California in 1999 and 2004, respectively. He worked as a Research Scientist with the Electrical Engineering and Computer Science Department, University of California, Irvine. He works as a Professor at the School of Electrical and Electronic Engineering, Yonsei University. Before joining Yonsei University, he worked as an assistant professor at the Department of Electrical and Computer Engineering, California State University, Northridge. His industry experience includes a college internship with Apple Computer, Inc., and a contract software engineer with ARM, Inc. His research interests include high-performance microprocessor design, GPU microarchitectures, neural network accelerators, and memory hierarchy design.

Abstract: In the ever-evolving landscape of computer systems and architecture, processing units remain at the core of technological innovation. This keynote embarks on a comprehensive journey through processing technologies' past, present, and future. We will begin by exploring the historical evolution and foundational role of Central Processing Units (CPUs) in advancing computational capabilities and system development. From there, we will delve into the rise of Graphics Processing Units (GPUs), highlighting their transformative impact on parallel processing and AI-driven applications. As we examine the current state of processing technologies, the keynote will spotlight cutting-edge developments that are pushing the boundaries of modern computing. This includes an overview of emerging architectures such as Neural Processing Units (NPUs) and other specialized accelerators reshaping performance and efficiency standards. We

will also discuss paradigm-shifting innovations like Processing-In-Memory (PIM) and in-storage computing, bringing computation closer to data to dramatically enhance performance and energy efficiency. The keynote will offer a forward-looking perspective on the next generation of processing technologies, including breakthroughs in quantum computing and the emergence of Quantum Processing Units (QPUs). Attendees will gain valuable insights into how these innovations will redefine the future of computing, with wide-ranging implications across industries such as healthcare, finance, entertainment, and beyond.

Wednesday, December 17 15:00 - 15:10 (Asia/Singapore)

CB5: Coffee Break

Room A, Room B, Boardroom

Wednesday, December 17 15:10 - 16:10 (Asia/Singapore)

A11: Operating System Platforms for Real-Time Embedded Applications

Track 11 Chair(s): M Norazizi Sham Mohd Sayuti, Universiti Sains Islam Malaysia, Malaysia

Room A

Real-time embedded applications demand operating systems that deliver deterministic performance, minimal latency, and robust resource management under stringent constraints. This session focuses on the design, implementation, and evaluation of operating system platforms tailored for multicore and manycore embedded systems. Topics include real-time scheduling, memory management, inter-core communication, mixed-criticality support, and OS-level virtualization. Presentations will highlight innovations that enhance predictability, scalability, and reliability across domains such as autonomous systems, industrial control, and mission-critical computing. The session aims to advance the state of real-time OS platforms as foundational enablers of responsive and dependable embedded intelligence.

A11.1 15:10 ***Efficient Load Balancing for On-chip Symmetric Multiprocessing through a Novel RTOS Approach for Multicore Microcontrollers***

Minjung Kim (Kyungpook National University, Korea (South)); Daejin Park (Kyungpook National University (KNU), Korea (South))

A11.2 15:25 ***Automated Deployment of Real-Time Tasks for Phased Execution on Scratchpad-Based Multicore Platforms***

Konstantin Dudzik and Maximilian Kirschner (FZI Research Center for Information Technology, Germany); Jürgen Becker (Karlsruher Institut für Technologie, Germany)

A11.3 15:40 ***Hetero-SplitEE: Split Learning of Neural Networks with Early Exits for Heterogeneous IoT Devices***

Yuki Oda, Yuta Ono, Hiroshi Nakamura and Hideki Takase (The University of Tokyo, Japan)

A11.4 15:55 ***Regular Expression Processing On A Many-Core Platform***

Sagar Sajeev and Bevan Baas (University of California, Davis, USA)

Wednesday, December 17 15:10 - 16:10 (Asia/Singapore)

B13: Embedded, Cyber-Physical, and IoT Systems

S-Session 13 Chair(s): Yiqin Xiang (Zhejiang University, China & University of Illinois Urbana-Champaign,USA), Xinghang Tan (Zhejiang University, China)

Room B

The fusion of embedded computing with cyber-physical and IoT technologies is driving innovation across smart environments, autonomous systems, and connected infrastructure. This session explores the design, integration, and deployment of multicore and manycore SoCs that enable intelligent sensing, control, and communication in dynamic, distributed settings. Topics include real-time data processing, edge computing frameworks, secure connectivity, and system-level co-design for responsiveness and reliability. Presentations will showcase solutions that bridge the digital and physical worlds, advancing the capabilities of embedded platforms in domains such as smart cities, healthcare, mobility, and industrial automation.

B13.1 15:10 ***A Nonvolatile IoT Sensor Node Based on Input-Data Driven Power-Gating Scheme and Its Emulation Using FPGA and Temperature Sensor***

Daisuke Suzuki (The University of Aizu, Japan); Takahiro Hanyu (Tohoku University, Japan)

B13.2 15:25 ***Detection of Avian Influenza-Infected Chickens using a Multi-Modal Audio-Visual Convolutional Neural Network Optimized for Indian Poultry Farms***

Mahadev A Gawas (State Higher Education Council, India & Directorate of Higher Education Goa, India); Hemprasad Yashwant Patil (Military College of Telecommunication Engineering, Mhow, India); Mridini M Gawas (Goa University, India & School of Physcial and Applied Sciences, India)

B13.3 15:40 ***Design and Implementation of a BRAM-Banked Double-Buffered Matrix Multiplication Accelerator for Transformer Models on Edge FPGAs***

Teo Tee Hui (Singapore University of Technology and Design, Singapore); Xinghang Tan (Zhejiang University, China)

B13.4 15:55 ***Development of Haul Truck Models for Testing Autonomous Safety in 1/14 Scale Test Mine***

Robert H Bissonette (NIOSH Spokane Mining Research Division, USA & Eastern Washington University, USA); Frank Lynch (EWU, USA); Michael C Meyer (Eastern Washington University, USA)

Wednesday, December 17 16:10 - 17:10 (Asia/Singapore)

A12: Application Domains for Embedded Multicore/Manycore SoCs

Track 12 Chair(s): Sweta Kumari (Shiv Nadar Institute of Eminence, India), Kaijie Wei (Keio University, Japan)

Room A

Embedded multicore and manycore System-on-Chips (SoCs) are powering a wide spectrum of application domains, from autonomous systems and smart healthcare to industrial automation

and immersive technologies. This session highlights how advanced SoC architectures are being tailored to meet the unique requirements of diverse fields, including performance, energy efficiency, real-time responsiveness, and reliability. Presentations will showcase domain-specific innovations, deployment strategies, and cross-layer optimization techniques that bridge hardware capabilities with software demands. The session aims to foster interdisciplinary dialogue and inspire new directions for embedded computing across emerging and mission-critical applications.

A12.1 16:10 ***Huffman Decoder for Baseline JPEG On Many-Core Platforms***

Derek S Li, Yechengnuo Zhang and Bevan Baas (University of California, Davis, USA)

A12.2 16:25 ***Scalable Discrete Cosine Transform Engines On A Many-Core Platform***

Michael Wang and Bevan Baas (University of California, Davis, USA)

A12.3 16:40 ***Accelerating Magnetic Particle Imaging with Data Parallelism: A Comparative Study***

Haipeng Zhu (Shenyang University of Technology, China); Yuan He (RIKEN Center for Computational Science, Japan & Keio University, Japan); Xiaohan Yue and Qinyang Zhang (Shenyang University of Technology, China); Lihui Wang (Soochow University, China); Shi Bai (Shenyang University of Technology, China)

A12.4 16:55 ***Mixed-precision backprojection using FP32 and FP64 for boosting satellite SAR imaging on embedded GPUs***

Masato Gocho and Masayoshi Tsuchida (Mitsubishi Electric Corporation, Japan); Kazunori Ueda (Waseda University, Tokyo, Japan)

Wednesday, December 17 16:10 - 17:10 (Asia/Singapore)

B14: Emerging Machine Learning and Deep Learning Models: Theory and Applications II

S-Session 14 Chair(s): Takao Tomono, Keio University, Japan

Room B

Rapid advances in machine learning and deep learning are reshaping the foundations of intelligent systems across disciplines. This session explores novel models, theoretical frameworks, and application-driven innovations that push the boundaries of learning algorithms and neural architectures. Topics include transformer-based models, graph neural networks, self-supervised learning, and hybrid approaches that integrate symbolic reasoning with statistical inference. Presentations will highlight breakthroughs in scalability, generalization, and domain adaptation, with applications spanning natural language processing, computer vision, scientific computing, and autonomous systems. The session aims to foster dialogue between theoretical development and practical deployment, accelerating the impact of learning technologies in embedded and distributed environments.

B14.1 16:10 ***Adaptive Calibration of Piezoresistive Pressure Sensors Across Variable Sensor Sizes***

Ratna Aisuwarya (Universitas Andalas, Indonesia & University of Aizu, Japan); Lei

Jing (University of Aizu, Japan)

B14.2 16:25 ***Advancing Dementia Prediction: A Robust CNN Framework for Early Diagnosis***

Md Farhadur Reza and Ali Kelly (Eastern Illinois University, USA)

B14.3 16:40 ***Smartwatch Design for Pedestrian Collision Detection***

Gowsiya Syednoor Shek (HTC Global Inc., USA); Salma Aga Shaik (San Jose State University, USA)

B14.4 16:55 ***P2P-Insole: Human Pose Estimation Using Foot Pressure Distribution and Motion Sensors***

Atsuya Watanabe (The University of Aizu, Japan & UoA I-Sensing Lab, Japan); Ratna Aisuwarya (Universitas Andalas, Indonesia & University of Aizu, Japan); Lei Jing (University of Aizu, Japan)

Wednesday, December 17 17:15 - 18:15 (Asia/Singapore)

A13: Hardware Acceleration of AI on Embedded Edge SoCs

Track 13 Chair(s): Sean Longyu Ma, The University of Auckland, New Zeeland

Room A

Delivering AI capabilities at the edge requires specialized hardware solutions that balance performance, power efficiency, and real-time responsiveness. This session focuses on architectural and implementation strategies for accelerating AI workloads on embedded multicore and manycore System-on-Chips (SoCs). Topics include custom accelerators for neural networks, reconfigurable computing, memory hierarchies, and co-design techniques that optimize inference and learning at the edge. Presentations will showcase innovations in low-power AI engines, dataflow architectures, and integration of machine learning frameworks into embedded platforms. The session aims to advance scalable, efficient, and intelligent edge computing through hardware-centric approaches.

A13.1 17:15 ***Energy-Efficient and Accurate Stochastic Computing-based Multiply-Accumulate Architecture for Neural Network Accelerator Design***

Chia-Heng Liu, Hsuan-Yu Huang, Bo-Chun Chen and Kun-Chih Chen (National Yang Ming Chiao Tung University, Taiwan)

A13.2 17:30 ***Random Forest-Based Approximation for Quantized CNNs on Edge FPGAs***

Yasuyuki Suzuki (University of Aizu, Japan); Hiroshi Saito and Shogo Semba (The University of Aizu, Japan); Yoichi Tomioka (University of Aizu, Japan); Takahiro Hanyu (Tohoku University, Japan)

A13.3 17:45 ***Instruction-Based Coordination of Heterogeneous Processing Units for Acceleration of DNN Inference***

Anastasios Petropoulos and Theodore A. Antonakopoulos (University of Patras, Greece)

A13.4 18:00 ***Design and Power-Efficiency Analysis of FPGA-based Dot and Outer Product Units***

Kyoji Awaki and Yoichi Tomioka (University of Aizu, Japan); Yuichi Okuyama, Hiroshi Saito and Shogo Semba (The University of Aizu, Japan); Stanislav Sedukhin (University of Aizu, Japan); Yuta Takahashi and Sumio Morioka (Interstellar Technologies Inc., Japan)

Wednesday, December 17 17:15 - 18:15 (Asia/Singapore)

B15: Parallel/Distributed, Grid, and Cloud Computing

S-Session 15 Chair(s): Zhishang Wang (The University of Aizu, Japan), Mahadev Gawas (Directorate of Higher Education Goa,India)

Room B

Scalable computing paradigms are essential to meet the demands of data-intensive and performance-critical applications across scientific, industrial, and commercial domains. This session explores the architectural, algorithmic, and deployment aspects of parallel, distributed, grid, and cloud computing systems. Topics include workload scheduling, resource orchestration, fault tolerance, virtualization, and energy-aware computing across heterogeneous platforms. Presentations will highlight innovations that leverage multicore and manycore technologies to enable high-throughput, resilient, and flexible computing infrastructures. The session aims to foster dialogue on bridging embedded systems with large-scale computing frameworks to support next-generation intelligent services.

B15.1 17:15 ***Carbon-Neutral Computing at the Edge: Scalable Greedy-LP Optimization of Green Data Centers***

Kazuki Okazawa, Hiroki Nishikawa, Dafang Zhao, Ittetsu Taniguchi and Takao Onoye (The University of Osaka, Japan); Marcos De Melo da Silva (France); Abdoulaye Gamatié (LIRMM (CNRS, University of Montpellier), France)

B15.2 17:30 ***OPT-MorphDAG: An efficient implementation of Directed Acyclic Graph (DAG)-Based Blockchain***

Anish Gupta, Sweta Kumari, Suryansh Rohil and Archit Somani (Shiv Nadar Institution of Eminence, India)

B15.3 17:45 ***From WiFi Signals to Skeletons: Accurate Multi-Person Pose Estimation with MPNet***

Weixiong Zhang, Weili Wang and Xuexuan Zhong (Guangzhou University, China); Lingjun Zhao (Guangdong Polytechnic Normal University, China); Qinglin Yang and Huakun Huang (Guangzhou University, China)

B15.4 18:00 ***Efficient WiFi-based Human Pose Estimation via Lightweight Model Design with Knowledge Distillation***

Weili Wang and Weixiong Zhang (Guangzhou University, China); Lingjun Zhao (Guangdong Polytechnic Normal University, China); Jiamin Yao, Qinglin Yang and Huakun Huang (Guangzhou University, China)

Wednesday, December 17 19:00 - 21:30 (Asia/Singapore)

K5-EHD: Conference Dinner, Evening Honorary Keynote & Best

Paper Award Announcement

Navigating the VUCA World: Reflections on Research, Education, and the Future of Work (Kiat Seng Yeo Singapore University of Technology and Design (SUTD), Singapore)

Room A, Room B

Biography: Kiat Seng Yeo (IEEE Fellow, F'16) is Advisor for Global Partnerships at SUTD, Director for Innovation and Enterprise (China), and Distinguished Professor at Tianjin University. With over 36 years in academia, industry, and consultancy, he has authored 14 books, 650+ papers, and holds 55 patents in low-power RF/mm-wave IC design and CMOS technology. He founded NTU's VIRTUS IC Design Centre, initiated SUTD's FIRST Industry Workshop, and secured over SGD70 million in research funding. His honors include Singapore's Public Administration Medal, Long Service Medal, and election to the Singapore Academy of Engineering and National Academy of Science. Recognized among the world's top 2% scientists (Stanford, 2020-2024), he is also named the world's top AI scientist by AIIA.

Abstract: The new challenges posed by the current VUCA (Volatility, Uncertainty, Complexity, Ambiguity) world, amplified by the rise of Artificial Intelligence (AI), would require a reimagination of how we structure our economy and address our future manpower needs. Countries must continue to invest in education and research to remain competitive. This talk begins with introducing a new education model in a new era. In addition, the fourth industrial revolution will change the world dramatically. The impact will be far more significant than its three predecessors. Specifically, many existing PMET (Professional, Manager, Executive, and Technician) jobs and traditional universities, technologies, and industries will disappear. Together with AI, they will shape and accelerate digital transformation and create new opportunities. The relationship between university and industry could take new forms in this new era. Their collaboration is increasingly important in developing new frontiers, ideas, knowledge, and growth areas. Finally, this talk will redefine research success and present new research areas. These rapid technological shifts will change how we think about research collaborations. It will also change the nature and direction of our research. What are the challenges of modern education and research? What are the next big things? How is it going to affect us? This talk will attempt to answer these questions.

Thursday, December 18

Thursday, December 18 9:00 - 10:00 (Asia/Singapore)

A14: Hardware Acceleration of AI on Embedded Edge SoCs II

Track 14 Chair(s): Mark Deutel (Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany), Sean Longyu Ma (The University of Auckland, New Zeeland)

Room A

Delivering AI capabilities at the edge requires specialized hardware solutions that balance performance, power efficiency, and real-time responsiveness. This session focuses on architectural and implementation strategies for accelerating AI workloads on embedded multicore and manycore System-on-Chips (SoCs). Topics include custom accelerators for neural networks, reconfigurable computing, memory hierarchies, and co-design techniques that optimize inference and learning at the edge. Presentations will showcase innovations in low-power AI engines, dataflow architectures, and integration of machine learning frameworks into embedded platforms. The session aims to advance scalable, efficient, and intelligent edge computing through hardware-centric approaches.

A14.1 9:00 *FPGA Implementation of Tiny Transformer Using High-Level-Synthesis for Biomedical Applications*

Teo Tee Hui (Singapore University of Technology and Design, Singapore); Mostafa Elsharkawy (Singapore University of Science and Technology, Singapore & Chang Gung University, Taiwan); I-Chyn Wey (Chang Gung University, Taiwan)

A14.2 9:15 *cpuC: a dynamic reconfigurable architecture for CNNs Acceleration*

Yosi Ben Asher (CS. University of Haifa, Israel & CS University of Haifa, Israel); Esti Stein (CS, Tel Aviv-Yaffo Academic College, Israel); Danial Jeres Jer (Israel); Ibrahim Qashqoush (University of Haifa, Israel); Roman Gilgor (Israel)

A14.3 9:30 *Multiplier-Free In-Memory Vector-Matrix Multiplication Using Distributed Arithmetic*

Felix Zeller and John Reuben (Friedrich-Alexander-Universität Erlangen-Nürnberg (FAU), Germany); Dietmar Fey (Chair for Computer Architecture, FAU, Erlangen, Germany)

A14.4 9:45 *An FPGA-Based Hardware-Software Co-Design Approach for Embedded Machine Learning Acceleration*

Obed K Allotey Babington and Nathan N Amanquah (Ashesi University, Ghana)

Thursday, December 18 9:00 - 10:00 (Asia/Singapore)

B16: Emerging Machine Learning and Deep Learning Models: Theory and Applications

S-Session Chair(s): Mudar Sarem (Faculty of Engineering, Manara University, Latakia, Syria), Ali Bostani (American University of Kuwait, Kuwait)

Room B, Boardroom

Rapid advances in machine learning and deep learning are reshaping the foundations of intelligent systems across disciplines. This session explores novel models, theoretical frameworks, and application-driven innovations that push the boundaries of learning algorithms and neural architectures. Topics include transformer-based models, graph neural networks, self-supervised learning, and hybrid approaches that integrate symbolic reasoning with statistical inference. Presentations will highlight breakthroughs in scalability, generalization, and domain adaptation, with applications spanning natural language processing, computer vision, scientific computing, and autonomous systems. The session aims to foster dialogue between theoretical development and practical deployment, accelerating the impact of learning technologies in embedded and distributed environments.

B16.1 9:00 *An Ensemble Virtual Metrology Model of Machine Learning in Semiconductor Manufacturing*

Ya Wei Chen (China Resources Microelectronics Limited, China & CRMicro, China); Shaohua Chang and Eric Chien (China Resources Microelectronics Limited, China)

B16.2 9:15 *Adaptive QoS to Handle Transient Overloads in Time-sensitive Vehicular Networks Caused by ADAS*

Leonardo Passig Horstmann, Antônio Augusto Fröhlich and Josafat Leal Filho (Federal University of Santa Catarina, Brazil); José Luis Conradi Hoffmann (Federal University of Santa Catarina & Software/Hardware Integration Lab, Brazil)

B16.3 9:30 ***Low-Cost Image Processing-Based Teleoperated Robotic Arm for Remote Surgical Assistance and Digital Health Integration***

Ali Bostani (American University of Kuwait, Kuwait & Microwavesoft, Kuwait)

B16.4 9:45 ***COPA: Cost and Performance Aware Traffic Engineering Framework in Multicloud SD-WAN***

Venkateswaran Dorai (Zscaler, USA)

Thursday, December 18 10:00 - 10:10 (Asia/Singapore)

CB6: Coffee Break

Room A, Room B, Boardroom

Thursday, December 18 11:10 - 12:10 (Asia/Singapore)

A15: Machine Learning for Energy-Efficient and Reliable Manycore Systems

Track 15 Chair(s): Md Farhadur Reza, Eastern Illinois University, U.S.A.

Room A

Machine learning is emerging as a powerful enabler for optimizing performance, energy efficiency, and reliability in manycore System-on-Chip (SoC) architectures. This session explores how learning-based techniques are being applied across the design and runtime spectrum to enhance system resilience, predict faults, manage power dynamically, and adapt to workload variations. Topics include predictive modeling, reinforcement learning for resource allocation, anomaly detection, and co-design strategies that integrate ML with hardware and software layers. Presentations will highlight innovations that reduce energy consumption, extend system lifetime, and ensure dependable operation in complex embedded environments.

A15.1 11:10 ***Implementation and Evaluation of Stable Diffusion on a General-Purpose CGLA Accelerator***

Takuto Ando, Yu Eto and Yasuhiko Nakashima (Nara Institute of Science and Technology, Japan)

A15.2 11:25 ***Neural Network-Based Mapping of Deep Neural Networks onto Network-on-Chip Architectures***

Md Farhadur Reza and Dominik R Cloud (Eastern Illinois University, USA)

A15.3 11:40 ***Adaptive Gradual Quantization with a Custom RISC-V SIMD Accelerator***

Zongcheng Yue, Dongwei Yan, Longyu Ma and Chiu Wing Sham (The University of Auckland, New Zealand)

Thursday, December 18 11:10 - 12:10 (Asia/Singapore)

B17: Edge-AI and Resilient SoC Design for Autonomous and Secure Systems

S-Session 17 Chair(s): Mark Deutel, Friedrich-Alexander-Universität Erlangen-Nürnberg, Germany

Room B

Autonomous and secure systems operating at the edge demand robust, intelligent, and energy-efficient computing platforms. This session explores the intersection of Edge-AI and resilient System-on-Chip (SoC) design, focusing on architectures and methodologies that ensure dependable performance in dynamic and often unpredictable environments. Topics include fault-tolerant hardware, secure execution models, adaptive learning at the edge, and co-design strategies for real-time responsiveness and cyber-physical integration. Presentations will highlight innovations that empower autonomous vehicles, robotics, and mission-critical IoT systems with embedded intelligence and system-level resilience. The session aims to advance the design of trustworthy, high-performance edge platforms for next-generation autonomous applications.

B17.1 11:10 ***robbit: a user-friendly and two-wheeled self-balancing robot using an FPGA***

Daichi Kumagai and Komei Kodera (Institute of Science Tokyo, Japan); Yuya Iwata (IBEX Technology Co. Ltd, Japan); Kenji Kise (Institute of Science Tokyo, Japan)

B17.2 11:25 ***Analytical Modeling of Task Allocation for Distributed Anthropomorphic Robots in Mission-Critical Environments***

Zhishang Wang (University of Aizu, Japan); Yassine Mohamed Khedher (The University of Aizu, Japan); Khanh N. Dang (University of Aizu, Japan); Michael Cohen (Higashi Nippon International University, Japan); Abderazek Ben Abdallah (The University of Aizu, Japan)

B17.3 11:40 ***F2MKDC: Fog-enabled Federated Learning with Mutual Knowledge Distillation and Clustering for Data Distribution-based Collaborative Learning***

Takuya Nomura (Saitama University, Japan); Yusuke Yamasaki (University of Tokyo, Japan); Shintaro Hosoai (Institute of Technologists, Japan); Hideki Takase (The University of Tokyo, Japan); Takuya Azumi (Saitama University, Japan)

B17.4 11:55 ***Evaluating Four FPGA-accelerated Space Use Cases based on Neural Network Algorithms for On-board Inference***

Pedro Nuno de Melo Antunes, Muhammad Ihsan Al Hafiz and Jonah Ekelund (KTH Royal Institute of Technology, Sweden); Panagiotis Gonidakis, Ekaterina Dineva and George Miloshevich (KU Leuven, Belgium); Artur Podobas (KTH, Royal Institute of Technology, Sweden)

Thursday, December 18 12:10 - 12:15 (Asia/Singapore)

C: Closing session

Program last updated on Dec 7