19TH INTERNATIONAL SYMPOSIUM ON EMBEDDED MULTICORE/MANY-CORE SYSTEMS-ON-CHIP

MCSoC-2026 · Final Program

December 14–17, 2026 · Shanghai Jiao Tong University, Shanghai

TIME ZONE
All times UTC+8
(Shanghai local time)

PAPER TALKS
15 min each
10 min talk + 5 min Q&A

CO-LOCATED SUMMITS NeuroCore Summit · Mon, Room A · EmbodiCore Summit · Wed, Room B · *mcsoc-forum.org*

Each paper is allotted 15 minutes (10-minute talk and 5 minutes of Q&A). The session chair and co-chair are listed under each session title, and the chair of each keynote is listed with the talk. Click a session title to go to its papers. The presenter of each paper is underlined.

Online participation (Zoom): Room A – Meeting ID **839 8259 2902** · Room B – Meeting ID **865 3881 0892**. The passcode and direct links are sent by email to registered authors and session chairs.

Time (China, UTC+8)	Room A	Room B
MONDAY, DECEMBER 14, 2026		
13:00–13:05	*O1: Kick-off Session*	
13:05–14:05	*K1: Keynote 1 – Hai Jin (Huazhong University of Science and Technology): A Unified Approach of Graph Computing* Session Chair: Tee Hui Teo (Singapore University of Technology and Design)	
14:10–15:10	**A1:** NeuroCore Summit I: Neuromorphic Circuits and Low-Power Devices	**B1:** S-Session 14: Advances in Intelligent Systems and Learning Technologies – I
15:10–16:10	**A2:** NeuroCore Summit II: Spiking Neural Networks and On-Chip Learning	**B2:** S-Session 14: Advances in Intelligent Systems and Learning Technologies – II
16:10–16:20	*Coffee/Tea Break*	
16:20–17:20	**A3:** NeuroCore Summit III: Brain-Inspired Algorithm–Hardware Co-Design and Applications	**B3:** S-Session 25: Governance-Aware Agentic AI for Systems-of-Systems
17:20–18:20	**A4:** NeuroCore Summit IV: Neuromorphic Accelerators and System Architectures	**B4:** S-Session 18: Harnessing AI Tools for Transforming Education
TUESDAY, DECEMBER 15, 2026		
09:00–09:20	*O2: Opening Session*	
09:20–10:20	*K2: Keynote 2 – Mingle Sun (Beijing SemiDrive Semiconductor Technology Co., Ltd.): Next-Generation AI SoCs for Automotive Applications and Embodied Intelligence: Meeting High-Performance, Multi-Task and Real-Time Requirements* Session Chair: Yongfu Li (Shanghai Jiao Tong University)	
10:20–10:40	*Coffee/Tea Break*	
10:40–12:10	**A5:** Hardware Acceleration of AI on Embedded Edge SoCs – I	**B5:** S-Session 1: Performance Optimization and Auto-Tuning of Software on Multicore/Manycore Systems (POAT2026)

Time (China, UTC+8)	Room A	Room B
12:10–13:30	*Lunch*	
13:30–14:30	*K3: Keynote 3 – Yan Xie (Li Auto): The Next Frontier of AI Inference: Why Dataflow is the Future of Intelligent Vehicles* Session Chair: Xinfei Guo (Shanghai Jiao Tong University)	
14:40–15:40	**A6:** Architectural Innovations in Embedded Multicore/Manycore SoCs – I	**B6:** Design Automation and Low-Power Techniques for Embedded Manycore SoCs
15:40–16:00	*Coffee/Tea Break*	
16:00–17:00	**A7:** Architectural Innovations in Embedded Multicore/Manycore SoCs – II	**B7:** Multicore SoCs for Cyber-Physical and Autonomous Systems – II
17:00–18:15	**A8:** Hardware Acceleration of AI on Embedded Edge SoCs – II	**B8:** Application Domains for Embedded Multicore/Manycore SoCs
WEDNESDAY, DECEMBER 16, 2026		
09:00–10:00	*K4: Keynote 4 – Mohamad Sawan (Westlake University): Brain-inspired SoC for Brain-Computer Interfaces and Embodied AI Applications* Session Chair: Zhishang Wang (The University of Aizu)	
10:00–10:15	*Coffee/Tea Break*	
10:15–11:15	**A9:** Design Methodologies for Embedded Multicore/Manycore SoCs – II	**B9:** S-Session 24: Human-Centric AI and Intelligent Systems for Sustainable Industry – I
11:15–12:30	**A10:** Hardware Acceleration of AI and Neuromorphic Edge Systems	**B10:** S-Session 24: Human-Centric AI and Intelligent Systems for Sustainable Industry – II
12:30–13:30	*Lunch*	
13:30–14:30	**A11:** Testing, Security, and Trust in Embedded Multicore/Manycore Systems – I	**B11:** Real-Time Systems for Embedded Multicore/Manycore SoCs
14:30–15:30	**A12:** Testing, Security, and Trust in Embedded Multicore/Manycore Systems – II	**B12:** Multicore SoCs for Cyber-Physical and Autonomous Systems – I
15:30–15:50	*Coffee/Tea Break*	
15:50–16:50	**A13:** S-Session 2: Emerging Machine Learning and Deep Learning Models: Theory and Applications	**B13:** EmbodiCore Global Summit on Embodied AI, Collaborative Humanoid, and Distributed Robotic Computing
18:30–21:30	*Dinner / Banquet*	
THURSDAY, DECEMBER 17, 2026		
09:00–10:00	**A14:** Testing, Security, and Trust in Embedded Multicore/Manycore Systems – III	**B14:** Machine Learning for Energy-Efficient and Reliable Manycore Systems
10:00–10:20	*Coffee/Tea Break*	
10:20–11:20	**A15:** Hardware Acceleration of AI on Embedded Edge SoCs – III	**B15:** Heterogeneous Integration and Advanced On-Chip Interconnects
11:20–12:20	**A16:** Design Methodologies for Embedded Multicore/Manycore SoCs – I	**B16:** Hardware Acceleration of AI on Embedded Edge SoCs – IV
12:20–12:40	*C: Closing Session*	

Sessions and Papers

Monday, December 14, 2026

A1: NeuroCore Summit I: Neuromorphic Circuits and Low-Power Devices

14:10–15:10 · Room A · Chair: Elishai Ezra Tsur (The Open University of Israel) · Co-chair: Pavan Nutalapati (Oracle Corp)

14:10	#128 **Beyond Static Power: Asynchronous vs Clock-Gated Integrate-and-Fire Layers in a Standard-Cell Flow** Zhanbo Shen (Eindhoven University of Technology); Henk Corporaal (Technical University Eindhoven); Sander Stuijk (Eindhoven University of Technology); Federico Corradi (TU Eindhoven)
14:25	#180 **Aging Analysis of CMOS Synaptic Circuits with Simplified Leaky Integrate-and-Fire Neurons** Jani Babu Shaik (Shanghai jiao tong university); Siona Menezes Picardo (Middlesex University Dubai); Fan Hu and Xinyue Wu (Shanghai Jiao Tong University); Sonal Singhal (Shiv Nadar University); Xinfei Guo (Shanghai Jiao Tong University)
14:40	#231 **From Python to Layout: The Spyqe Framework for Generating Asynchronous Neuromorphic Circuits** Zhanbo Shen and Sander Stuijk (Eindhoven University of Technology); Federico Corradi (TU Eindhoven)
14:55	#240 **Resilient On-Chip STDP Learning Under Memory Voltage Scaling for Ultra-Low-Power Neural Network Processors** Subbaiah Ravi Hariprakash and Yuga Hanyu (University of Aizu); Abderazek Ben Abdallah (The University of Aizu); Zhishang Wang and Khanh N. Dang (University of Aizu)

B1: S-Session 14: Advances in Intelligent Systems and Learning Technologies – I

14:10–15:10 · Room B · Chair: Mohamed Badawy (Infineon Technologies AG & Technical University of Munich) · Co-chair: Sandeep Sonawane (Nutanix Inc.)

14:10	#131 **Residual Deep Neural Network for Explainable Student Academic Performance Classification** Yousuf Nasser Al Husaini and Mohammed Abdulla Salim Al Husaini (Arab Open University); Mohammad Abrar (Arab Open University)
14:25	#148 **Interpretable Hidden-State Modeling of Programming Learning Progression** Md. Shahajada Mia (The University of Aizu); Yutaka Watanobe (University of Aizu); Md Mostafizer Rahman (University of Notre Dame); Md Faizul Ibne Amin and Daniel Muepu Mukendi (The University of Aizu)
14:40	#307 **Score Agreement and Confidence Calibration in Grounded LLM Short-Answer Scoring** Anoop Yadav, Muhammad Jawad Arshad and Yutaka Watanobe (University of Aizu)
14:55	#216 **Codiflect: An Intelligent Tutoring System for Idiomatic Python with RAG-Based LLM Tutorials and Deterministic Selection and Verification** Jonas Sobotta and Li Ke (University of Aizu); Mohamed Hamada (UoA); Yutaka Watanobe (University of Aizu)

A2: NeuroCore Summit II: Spiking Neural Networks and On-Chip Learning

15:10–16:10 · Room A · Chair: Elishai Ezra Tsur (The Open University of Israel) · Co-chair: Vijayakumar Venganti (Cisco Systems, Inc.)

15:10	#71 **MSTDP-Trained Izhikevich Spiking Neural Networks for Reinforcement Learning** Tuan-Hung Nguyen, Khanh Ngoc Nguyen and Nam Hai Nguyen (University of Transport and Communications); Quang Huy Dong (University of Transportation and Communication); Truong Cong Tan (Trường Đại Học Giao Thông Vận Tải); Truong Duc Phuong (University of Transport and Communications); Khanh N. Dang (University of Aizu); Duy-Anh Nguyen (University of Transport and Communications)
15:25	#139 **Event-Driven Language Models with Sparse Neural Activity for Neuromorphic Hardware** Simon Richter (University of Southern Denmark - SDU); Ruhai Lin (University of California, Santa Cruz); Jason Yik (Harvard University); Taylor Kergan and Rui-Jie Zhu (University of California, Santa Cruz); Farshad Moradi (University of Southern Denmark); Jason K. Eshraghian (University of California, Santa Cruz)

15:40	#160 **IzhiGAN: A Calibration Aware ANN to SNN Framework for Efficient Image Generation** Quang-Thai Pham, Thanh-Dat Nguyen, Van-Vu Luyen and Duy-Anh Nguyen (University of Transport and Communications); Yuga Hanyu and Khanh N. Dang (University of Aizu)
15:55	#272 **A Spiking Trajectory Memory for Predicting Repetitive Motion from Event Cameras** Sagi Taizi and Elishai Ezra Tsur (The Open University of Israel)

B2: S-Session 14: Advances in Intelligent Systems and Learning Technologies – II

15:10–16:10 · Room B · Chair: Yousuf Nasser Al Husaini (Arab Open University) · Co-chair: Somesh Rahul (Independent Researcher)

15:10	#264 **Digital-Twin-Driven Experiential Learning for Cyber-Physical Security: Teaching Zero Trust Through Real-Time Industrial Process Consequences** Abdul Khadir Mahamed, Ramesh Subramani and Sai Pavan Kumar Mandapaka (New York University)
15:25	#332 **Code Refactoring with LLM: A Comprehensive Evaluation Across Few-Shot Settings** Md. Raihan Tapader (Dhaka University of Engineering & Technology, Gazipur); Md Mostafizer Rahman (University of Notre Dame); Ariful Islam Shiplu, Md Faizul Ibne Amin and Md. Shahajada Mia (The University of Aizu); Yutaka Watanobe (University of Aizu)
15:40	#169 **An LLM-Driven Multi-Agent Intelligent System for Autonomous Smart Home Management** Akila Siriweera (University of Aizu); Janani Rangila (Kotelawala Defence University)
15:55	#168 **Automated IELTS Diagnostic Assessment for L1 Sinhala Speakers via Retrieval-Grounded Dual-Rater LLM Scoring with Official Band Descriptors** Akila Siriweera (University of Aizu); Vishmika Devindi (KDU University)

A3: NeuroCore Summit III: Brain-Inspired Algorithm–Hardware Co-Design and Applications

16:20–17:20 · Room A · Chair: Elishai Ezra Tsur (The Open University of Israel) · Co-chair: Chandrashekhar Medicherla (Salesforce Inc)

16:20	#279 **Investigating the Impact of Mapping-Awareness in Hardware-Aware Spiking Neural Architecture Search** Hella Toto Kiesa and Jonas Bergmann (Karlsruhe Institute of Technology); Sven Nitzsche (FZI Forschungszentrum Informatik); Tanja Harbaum and Juergen Becker (Karlsruhe Institute of Technology)
16:35	#82 **An Energy-efficient BitNet LLM Accelerator with a Reconfigurable Bit-cascaded MAC Core and 1.6-bit Online Weight Decompression** Chaoming Fang, Ziyang Shen and Jie Yang (Westlake University); Mohamad Sawan (Westlake University & Polytechnique Montréal)
16:50	#38 **Next-Generation Neurotechnology AI-Augmented Systems for Emotional & Cognitive Enhancement** Manish Meshram (Crave Infotech); Sparsh Potti (Research Assistant)
17:05	#164 **A Resource-Efficient Deepfake Images Detection Pipeline Utilizing Lightweight Convolutional Neural Networks** Rasel Ahmed Raju, Zeba Tashin Oeeshee, Md. Rakibul Islam Reshad and Muhammad Shafayat Oshman (North South University)

B3: S-Session 25: Governance-Aware Agentic AI for Systems-of-Systems

16:20–17:20 · Room B · Chair: TBC · Co-chair: Abdul Khadir Mahamed (New York University)

16:20	#145 **AI Ambassadors: A Governance-Aware Agentic AI Framework for Trusted and Autonomous Consular Service Delivery in Digital Embassies** Mohammed Saeed Jawad (International University of Sarajevo); Marcin Mrugalski (University of Zielona Góra); Taher Alzahrani (Imam Mohammad Ibn Saud Islamic University (IMSIU)); Dino Kečo; Mohammad Al-Johani (International Burch University (IBU))
16:35	#300 **SPARKI: Evidence-Contract Support for Governed AI-Assisted Engineering Workflows** Chad Curbow and Michael C Meyer (Eastern Washington University)

16:50	#306 **PAGER: Policy-Aware Routing and Agent Selection for Multi-Agent Systems** Siva Kumar Chintham (LTM); Seema Gangaiah Aarella (Austin College & University of North Texas); Atul Prasad (University of San Diego); Shomik Basu (Workday Inc); Sai Srinivas Choudary Potla (Innovaccer); Pratik Bundela (IEEE); Akshay Deshpande (Waymo); Shiva Kumar Devalokam Subrayappa (Evernorth Health Services)
17:05	#309 **Authorization-Aware Detection of Indirect Prompt Injection in Retrieval-Augmented Generation** Aswathnarayan Muthukrishnan Kirubakaran (Meta Inc); Pratik Bundela (IEEE); Ram Sekhar Bodala (Amtrak); Akshay Deshpande (Waymo); Murali Shankar Dulam (JPMorgan Chase); Suhas Malempati (MetaDigi Labs Inc); Anurag Kumar (Cisco Systems); Nitin Saksena (Albertsons Companies)

A4: NeuroCore Summit IV: Neuromorphic Accelerators and System Architectures

17:20–18:20 · Room A · Chair: Elishai Ezra Tsur (The Open University of Israel) · Co-chair: Siddhant Bapusaheb Tanpure (Meta)

17:20	#92 **SCDQ: A Shared Circular Delay Queue for Scalable Synaptic Delays in Neuromorphic Accelerators** Roy Meijer (Eindhoven University of Technology); Paul Detterer (IMEC-NL); Amirreza Yousefzadeh (University of Twente); Alberto Patino-Saucedo (IMSE); Guangzhi Tang (Maastricht University); Kanishkan Vadivel (IMEC); Yingfu Xu (IMEC-NL); Manil Dev Gomony (Eindhoven University of Technology); Federico Corradi (TU Eindhoven); Bernabe Linares-Barranco (Instituto de Microelectronica de Sevilla); Manolis Sifalakis (Innatera)
17:35	#99 **A Low-Cost FPGA Implementation of a Time-Division-Multiplexed Spiking Neural Network** Marwan Ahmed Elsayed Fetteha and Ameer Abdelhadi (McMaster University)
17:50	#68 **The Sparsity Tax: Weight Sparsity Trade-offs in Event-Driven SIMD and SIMT Neuromorphic Cores** Mattias Westerink, Sameed Sohail, Berend Jan van der Zwaag, Sabih H. Gerez and Amirreza Yousefzadeh (University of Twente)
18:05	#119 **An Event-Driven Asynchronous Multi-Lane Serial Interconnect for Chiplet-Scale Neuromorphic Integration** Sameed Sohail, Douwe De Vries, Berend Jan van der Zwaag, Sabih H. Gerez, Ana Lucia Varbanescu and Amirreza Yousefzadeh (University of Twente)

B4: S-Session 18: Harnessing AI Tools for Transforming Education

17:20–18:20 · Room B · Chair: Yousuf Nasser Al Husaini (Arab Open University) · Co-chair: Youngsoo Kim (University of Minnesota Duluth)

17:20	#149 **Hybrid FPGA-Based Random Number Generator Using Linear Feedback Shift Registers, Thermal Noise Injection, Von Neumann Correction, and Nonlinear Post-Processing for Conway's Game of Life Visual Display** Teo Tee Hui, Vincent Ho and Khant Htet Kaung (Singapore University of Technology and Design); Binghe Li (ZJU-UIUC Institute, Zhejiang University, Haining); Rey Lam, Jeremiah He, Logavarshini Kandaraj and Kulkarni Ojas Jaydeep (Singapore University of Technology and Design)
17:35	#150 **Novel Interactive Reaction Game Design Incorporating Real-Time FPGA-Based Multiple-Recursive Pseudo-Random Number Generator for Psychomotor Training** Teo Tee Hui, Zhao En Koh, Hoi Chia, Renzo Ricardo King, Francine Flores Casana and Joel Yeo (Singapore University of Technology and Design); Yifei Yang (University of Waterloo); Bo Wen Heng (Singapore University of Technology and Design)
17:50	#151 **Design and Implementation of a Correlation-Aware Digital Shaker System for Pseudo-Random Number Generation Using Piezoelectric Sensing and Congruential Generators** Teo Tee Hui, Harsh Agarwal and Benjamin Lee (Singapore University of Technology and Design); Vanessa Slavov (University of Waterloo); Sanika Kalyan Sonpethkar, Mohamed Danial B Hamdan and Aryan Gupta (Singapore University of Technology and Design)
18:05	#152 **Programmable Anomaly Detector System: An Embedded, Real-Time IoT Acoustic Fault Detection using Hybrid FFT, CNN Autoencoder on a Resource Constrained FPGA** Teo Tee Hui and Gavin Tan (Singapore University of Technology and Design); Eric Aleong (University of Waterloo); Keming Su, Wesley Teo and Haneeshwar Reddy (Singapore University of Technology and Design)

Tuesday, December 15, 2026

A5: Hardware Acceleration of AI on Embedded Edge SoCs – I

10:40–11:55 · Room A · Chair: Mushtaq Ahmed (Malaviya National Institute of Technology Jaipur) · Co-chair: Md Farhadur Reza (Eastern Illinois University)

10:40	#87 **Mamba-Family State-Space Model Kernels on a Programmable CGLA** Takuto Ando and Yasuhiko Nakashima (Nara Institute of Science and Technology)
10:55	#162 **FPGA Implementation and Performance Evaluation of Memory-Loaded Ternary Linear Layers under Varying Sparsity** Ryota Kayanoma and Hiroki Nakahara (Tohoku University); Yumiko Uchida and Yoshitaka Miyatani (Sony Semiconductor Solutions Corporation)
11:10	#123 **Accuracy-Aware, Hardware-Adaptive Co-Optimization of Pruning and Dataflow Mapping for Modern DNNs** Md Farhadur Reza (Eastern Illinois University)
11:25	#171 **CNN-Based Many-Core Single-Image Super-Resolution** Pei Yun Chen and Bevan Baas (University of California, Davis)
11:40	#313 **Accelerating Sparse Matrix-Vector Multiplication on Ryzen XDNA2 NPU** Hitoshi Komurasaki (The University of Tokyo); Masayuki Usui (Tokyo University); Takatsugu Ono (Kyushu University); Shinya Takamaeda-Yamazaki (The University of Tokyo & RIKEN)

B5: S-Session 1: Performance Optimization and Auto-Tuning of Software on Multicore/Manycore Systems (POAT2026)

10:40–12:10 · Room B · Chair: Siva Kumar Chintham (LTM) · Co-chair: TBC

10:40	#81 **Neural-Guided Warm Starts for Digital Annealing of Large-Scale QUBO Problems** Yu Ting Chen, Yu-Ru Pai and Yu-Chen Shu (National Cheng Kung University)
10:55	#172 **Benchmark-Guided Selection of Managed, Prefetched, and Manual GPU-to-GPU Migration** Masatoshi Kawai (Tohoku University); Satoshi Ohshima (Kyushu University); Hiroyuki Takizawa (Tohoku University)
11:10	#220 **A Branch-Free General Renormalization Scheme for Pair Arithmetic and Its Performance Evaluation** Tomonori Kouya (Otemon Gakuin University)
11:25	#282 **Degrees of Freedom in Submit-Time HPC Job Power Prediction: A Measurement Study** Haoran Ding, Sichen Tao, Masatoshi Kawai and Hiroyuki Takizawa (Tohoku University)
11:40	#294 **Virtual Threads on a Heterogeneous Multicore SoC: An Empirical Study of Java Thread-per-Connection Servers under I/O, CPU and Synchronization Load** Udaya Bhasker Mattupalli (Accenture); Ayaskant Pattnaik and ShravanKumar Arram; Krishnaprasad Chouty (Sophlogic Global LLC); Dinesh Babu Mannu (Fidelity Investments); Balamurugan Chelladurai (Wipro Technology); Naresh Kumar Sankar Kumar
11:55	#297 **Accuracy at a Cost: Efficiency-Performance Trade-offs in Recurrent and Attention-Based Code Models** Muhammad Jawad Arshad, Anoop Yadav, Timur Jaganov and Yutaka Watanobe (University of Aizu)

A6: Architectural Innovations in Embedded Multicore/Manycore SoCs – I

14:40–15:40 · Room A · Chair: Mushtaq Ahmed (Malaviya National Institute of Technology Jaipur) · Co-chair: Siva Prasad Nandi (Oracle America Inc.)

14:40	#114 **IAIP: Interrupt-Aware Instruction Prefetcher** Tim Twardzik and Lars Nolte (Technische Universität München); Thomas Wild and Andreas Herkersdorf (Technical University of Munich)
14:55	#113 **HENDAL: Hardware-Assisted Early Notification for Event-Driven Applications in Linux** Lars Nolte and Tim Twardzik (Technische Universität München); Marco Liess, Thomas Wild and Andreas Herkersdorf (Technical University of Munich)

15:10	#167 **Buffer Designs for Dynamic Scheduling of Mixed-Latency Operations** Demyana Emil Mekhail Selim and Klaus Schneider (RPTU Kaiserslautern-Landau)
15:25	#315 **Memory Admission and Result-Retention Sizing in an RV32IMC FPGA Soft Processor** Yihang Dai, Shuyu Xu, Yinfeng Zhou and Chenglei Peng (Nanjing University)

B6: Design Automation and Low-Power Techniques for Embedded Manycore SoCs

14:40–15:40 · Room B · Chair: Jani Babu Shaik (Shanghai Jiao Tong University) · Co-chair: Sandeep Shivam (Independent Researcher)

14:40	#198 **Thermal-Aware Floor Planning Under Process Variation Using Reinforcement Learning for 3D-IC Microelectronics** Md. Ariful Islam Bhuiyan (California State University, Northridge); Dipta Roy, Kazi Mushfiq Rafid, Raj Kumar and Somnath Chattopadhyay (California State University Northridge)
14:55	#177 **CARDAMOM: Cycle-Accurate RISC-V Dynamic Method for Power Prediction using Attention Mechanisms** Ameya Ramteke (Birla Institute of Technology and Science); Paresh Saxena (BITS Pilani); Soumya J (BITS Pilani, Hyderabad Campus); Ankit Agrawal and Shankar Ramakrishnan (Google LLC)
15:10	#268 **Low-Power FPGA Implementation of Adaptive Line Enhancers Using Reduced-Precision Arithmetic for SoC-Based IoT and Neural-Computing Applications** Hen-Geul Yeh (California State University Long Beach); Brian Pham and Ryan Chang (California State University, Long Beach)
15:25	#239 **A Capacitance-Aware Training Framework for Decision Tree Inference Circuits** Woramet Janchum and Thanasin Bunnam (Rajamangala University of Technology Thanyaburi); Pitchayapatchaya Srikram (RMUTT)

A7: Architectural Innovations in Embedded Multicore/Manycore SoCs – II

16:00–17:00 · Room A · Chair: TBC · Co-chair: Rashmi Prabhakar Sarode (Indian Institute of Technology Madras)

16:00	#158 **An On-Chip Supervisor Architecture for the Configuration, Diagnosis, and Debug of High-Speed Communication Datapaths** Federico I. Villar (Fundación Fulgor); Ariel Pola (Fundación Fulgor); Pablo S. Mandolesi (Universidad Nacional del Sur)
16:15	#285 **COMET: A Lightweight Rate-Portable Ethernet Remote-Memory Engine for Heterogeneous FPGA Systems** Keisuke Takano (Japan Advanced Institute of Science and Technology); Akira Uejima (Okayama University of Science); Yasushi Inoguchi (Japan Advance Institute of Science and Technology)
16:30	#211 **Dual-Anchor Calibration and Design Space Exploration of the Open-Source RISC-V Core C910 for Embedded IoT Workloads** Ze Hong (The 58th Research Institute of China Electronics Technology Group); Zilin Wang, Huiwang Zhou and Zhenjiao Chen (The 58th Research Institute of China Electronics Technology Group)
16:45	#224 **A Tri-mode Drop-K Sequential Backward Selection Architecture and Implementation** Hsuan-Fu Liu, Tao Jung Wang, Lan-Da Van, Hui-chun Tseng and Chen Wei Liao (National Yang Ming Chiao Tung University); Chun-Ming Huang (Taiwan Semiconductor Research Institute, National Institutes of Applied Research); Tzyy-ping Jung (UCSD)

B7: Multicore SoCs for Cyber-Physical and Autonomous Systems – II

16:00–17:00 · Room B · Chair: TBC · Co-chair: Abdul Khadir Mahamed (New York University)

16:00	#159 **Hardware-Assisted Event-Driven Temperature Monitoring on a LiteX-Based RISC-V SoC** Daisuke Suzuki (The University of Aizu); Takahiro Hanyu (Tohoku University)
16:15	#274 **Delaunay-Seeded Column Generation for Coverage-Constrained Sensor Augmentation** Ali Suliman Alsalehy (Jubail Industrial College)
16:30	#303 **Branch Pruning in Graph-Based Video Summarization: Fewer Branches, Lower Latency on Edge Devices** Yu Wang, Tom White and Dakota Sterling (Gonzaga University); Yujie Li (Guilin University of Electronic Technology); Michael C Meyer (Eastern Washington University)

16:45	#86 **NAS-DNM: Neural Architecture Search for Dendritic Neuron Modeling in VA-ECMO Mortality Prediction** Bingchao Shi (Hirosaki University); Sichen Tao (Tohoku University); Ruihan Zhao (Tongji University); Hanyu Hu (China University of Petroleum); Sicheng Liu (Yantai Vocational College); Yifei Yang (Hirosaki University)

A8: Hardware Acceleration of AI on Embedded Edge SoCs – II

17:00–18:00 · Room A · Chair: TBC · Co-chair: Somesh Rahul (Independent Researcher)

17:00	#98 **LiteBear: A Robust and Efficient FPGA-Based Bearing Fault Diagnosis System** Jianglan Zhu, Yulin Fu, Jiale Li, Longyu Ma and Chiu Wing Sham (The University of Auckland)
17:15	#108 **A Robust PYNQ-Based Runtime for Partially Reconfigurable CNN Inference on Zynq MPSoC** Yuhui Jiang, Hitesh B, Sheral Crescent Tissera and Rajesh C Panicker (National University of Singapore)
17:30	#112 **Accelerating CNN on FPGA for Real-time Object Detection in Defense Applications** Adithya R Prabhu, Kevin Jose and Kala S (Indian Institute of Information Technology Kottayam)
17:45	#202 **An FPGA-Based CNN Accelerator Architecture Using Line-Buffer Layer Fusion for ADAS Applications** Jeonghun Im (Santa Clara University); Radhika Grover (Santa Clara University & Member, Frugal Innovation Lab, Santa Clara University)

B8: Application Domains for Embedded Multicore/Manycore SoCs

17:00–18:15 · Room B · Chair: Zhishang Wang (The University of Aizu) · Co-chair: Abdul Khadir Mahamed (New York University)

17:00	#210 **Metadata-Aware Policy Enforcement for Secure Enterprise Data Lakes** Murali Shankar Dulam (JPMorgan Chase); Darshan Mohan Bidkar (IEEE); Mythili Annamalai Sekar (Amazon Inc); Siva Kumar Chintham (LTM); Naga Surya Kamala Dattatreya Pasupuleti (JPMorgan Chase); Shiva Kumar Devalokam Subrayappa (Evernorth Health Services); Narender Reddy Bitla (JPMorgan Chase); Bikesh Kumar (Apple Inc.)
17:15	#325 **Adaptive Push-Down Query Optimization Under Multi-Cloud DoS Attacks** Nachiappan Chockalingam (Meta); Shomik Basu (Workday Inc); Sai Srinivas Choudary Potla (Innovaccer); Sumit Saha (East West Bank); Ashok Gadi Parthi (None); Mayilsamy Palanigounder (NTT Data); Akash K Agarwal (Albertsons Companies Inc); Atul Prasad (University of San Diego)
17:30	#280 **Multicore Processing for Scalable Execution Layer in Secure Online Examination Systems** Rashmi P Sarode (Indian Institute of Technology, Madras); Yutaka Watanobe (University of Aizu); Subhash Bhalla (IIT Delhi)
17:45	#331 **Adaptive Walsh-Hadamard Precoding and Opportunistic Reception for Reliable Uplink OFDM-NOMA** Ravinder Singh (Malaviya National Institute of Technology Jaipur); Mushtaq Ahmed (Malaviya National Institute of Technology Jaipur INDIA); Mehwish Qureshi and Aryan Pingoliya (MNIT Jaipur); Rajendra Prasad Yadav (Malaviya National Institute of Technology Jaipur)
18:00	#322 **Hardware-Acceleration of Advanced Precoding for mMIMO 5G/6G Systems on RISC-V vDSPs** Javier Acevedo (Technical Univierstiy of Dresden); Patrick Seeling (Central Michigan University); Frank H.P. Fitzek (Technische Universität Dresden & ComNets - Communication Networks Group)

Wednesday, December 16, 2026

A9: Design Methodologies for Embedded Multicore/Manycore SoCs – II

10:15–11:15 · Room A · Chair: TBC · Co-chair: Youngsoo Kim (University of Minnesota Duluth)

10:15	#135 **End-to-End Memory Design Automation: From Behavioral Specifications to Platform-Specific Implementation** Mohamed Badawy (Infineon Technologies AG & Technical University of Munich); Hari Sankar Sahasranaman (Infineon Technologies AG, Technical University of Dresden); Wolfgang Ecker (Infineon Technologies AG)
10:30	#121 **Exploring Energy-Efficient Accelerator for Pyramidal Lucas-Kanade Optical Flow Algorithm via Processing Element Optimization** Zhifei Liu and Shogo Semba (The University of Aizu); Yoichi Tomioka (University of Aizu); Hiroshi Saito (The University of Aizu)
10:45	#225 **Performance Estimation and Algorithmic Transformation for Filtering Accelerator using FPGAs** Youngsoo Kim (University of Minnesota at Duluth)
11:00	#133 **PIMScope: Augmenting Ramulator 2.0 with Command-Level LPDDR-PIM for Transformer Inference** Ting Lin and Runxi Wang (Shanghai Jiao Tong University); Jani Babu Shaik (Shanghai jiao tong university); Xinfei Guo (Shanghai Jiao Tong University)

B9: S-Session 24: Human-Centric AI and Intelligent Systems for Sustainable Industry – I

10:15–11:15 · Room B · Chair: Siva Kumar Chintham (LTM) · Co-chair: Aswathnarayan Muthukrishnan Kirubakaran (Meta Inc.)

10:15	#48 **Event Contract Drift Detection and Impact Analysis in Enterprise Event-Driven Integration Systems** Siva Rama Krishna Varma Bayyavarapu (Senior IEEE Member); Srinivasateja Songa (The Home Depot); Siva Prasad Nandi (Oracle); Krishna Suman Dara (None); Raghuram Malpe Pai (HPE Networking)
10:30	#259 **Binding Drift: Latent Conflicts in Intent-Based Networks** Krishna Suman Dara, Raghuram Malpe Pai, Somesh Rahul, Mohammed Kamran Syed, Amarnath G S and Shivaprasad Gali (Independent Researcher)
10:45	#260 **CertiSense: Certified Telemetry Acquisition for Learned Anomaly Detection under a Quality Budget** Raghuram Malpe Pai, Krishna Suman Dara, Somesh Rahul, Amarnath G S, Anudeep Rentala and Shivaprasad Gali (Independent Researcher)
11:00	#84 **AIQEA: An Autonomous AI-Driven Quality Embedding Architecture** Vinil Pasupuleti (IBM); Koushik K Ganeeb (Salesforce); Shyalendar Reddy Allala (Global Atlantic Financial Company); Siva Rama Krishna Varma Bayyavarapu (Senior IEEE Member); Srinivasateja Songa (The Home Depot); Shrey Tyagi (Salesforce Inc)

A10: Hardware Acceleration of AI and Neuromorphic Edge Systems

11:15–12:30 · Room A · Chair: Tee Hui Teo (Singapore University of Technology and Design) · Co-chair: Ananda Biswas (Iowa State University)

11:15	#219 **A Zero-DSP Binarized Convolutional Neural Network on MNIST Digit Recognition on FPGA** Yuxuan Jiang (University of Electronic Science and Technology of China)
11:30	#261 **A Linux-Capable FPGA Heterogeneous SoC with an Out-of-Order LoongArch Core and NPU for Multimodel Edge Inference** Zigian Chen (Beihang University)
11:45	#299 **FLEXN: M-Flexible Low-cost EXecution of N: M Sparsity for DNNs** Ozgur Ozerdem and Alex Orailoglu (UC San Diego, Computer Science and Engineering)
12:00	#104 **Reducing Instruction-Fetch Energy in RISC-V for Embedded AI Processing via Dynamic and Static Loop Caching** Wiebren Wijnstra, Sameed Sohail, Berend Jan van der Zwaag, Sabih H. Gerez and Amirreza Yousefzadeh (University of Twente)
12:15	#176 **A Low-Power Spiking Neural Network on FPGA for EEG Motor Imagery Classification** Tahir Towsif and Arash Ahmadi (Carleton University)

B10: S-Session 24: Human-Centric AI and Intelligent Systems for Sustainable Industry – II

11:15–12:15 · Room B · Chair: Zhishang Wang (The University of Aizu) · Co-chair: Aswathnarayan Muthukrishnan Kirubakaran (Meta Inc.)

11:15	#47 **Federated NLP with Cross-Attention Transformers for Climate-Regulatory Risk Analytics in Banking** Rohit Nimmala (Bank of America); Madhushree Kumari (IEEE Senior Member); Jagrut Nimmala (Lowes Companies)
11:30	#316 **MAESTRO: A Multi-Agent, Evolving-memory System with Tool-grounded Reasoning and Orchestration Harness for PLC Code Generation** Mudar Sarem (Manara University); Tarek Jurdi (Tishreen University); Laya Albshlawy (Gen. Org of Remote Sensing); Ebrahim Massrie (Osmania University)
11:45	#251 **Anchored Chromatic Normalisation for Camera-Based Virtual Try-On: A Spectral Study of White Balance and Colour Fidelity Across Skin Tones** Somesh Rahul, Krishna Suman Dara, Raghuram Malpe Pai, Mohammed Kamran Syed and Anudeep Rentala (IEEE Independent Researcher)
12:00	#277 **Adaptive Multimodal Fusion for Robust Hazard Detection on a Low-Cost Embedded Platform** Bo Wen Heng and Teo Tee Hui (Singapore University of Technology and Design); I-Chyn Wey (Chang Gung University); Chiang Liang Kok (The University of Newcastle Australia)

A11: Testing, Security, and Trust in Embedded Multicore/Manycore Systems – I

13:30–14:30 · Room A · Chair: Jani Babu Shaik (Shanghai Jiao Tong University) · Co-chair: Murali Shankar Dulam (JPMorgan Chase & Co.)

13:30	#163 **Stealthy Black Hole Router Attacks in Network-on-Chip: Autoencoder-Based Detection with Adaptive DyXY Routing Mitigation** Dilshad Mohammed, Bhavya R and Adersh A (NSS College of Engineering, Palakkad); Adeela Farshana A and Syam Sankar (NSS College of Engineering, Palakkad)
13:45	#51 **A-DSRM-SEC: An Agile-Infused Design Science Research Methodology for Security Artifact Development in Embedded Multicore/Manycore Systems** Jovita Nsoh (University of Houston & Google)
14:00	#288 **GovAgent: Stateful, Auditable Policy Enforcement for Enterprise AI Agents on Multicore Processors** Udaya Bhasker Mattupalli (Accenture); Ayaskant Pattnaik, Nagaraju Akkuledu Uppara, Gangadhara Raghu Kopparapu and ShravanKumar Arram; Krishnaprasad Chouty (Sophlogic Global LLC)
14:15	#320 **GHOST: GNN-powered Attacks on Hardware Accelerator Obfuscation at RTL** Srinivasa Rao Dara (IDRBT & NITW); Dipanjan Roy (IDRBT Hyderabad); Ilaiah Kavati (National Institute of Technology Warangal)

B11: Real-Time Systems for Embedded Multicore/Manycore SoCs

13:30–14:15 · Room B · Chair: TBC · Co-chair: Raghuram Malpe Pai (HPE Networking)

13:30	#110 **Compilation of Neural Networks for Time-Predictable Multicore Processors with Local Memories** Maximilian Kirschner and Marius Kreutzer (FZI Research Center for Information Technology); Juergen Becker (Karlsruhe Institute of Technology)
13:45	#245 **ePMD-TT: Placeholder-based Mixed-Criticality Deployment of Event-triggered Anytime Neural Networks into Time-triggered Periodic Schedules** Matthias Stammler (Karlsruhe Institute of Technology); Felix Frombach (Karlsruher Institut für Technologie); Patrick Schmidt (Karlsruhe Institute of Technology); Federico Gavioli (Universita di Modena e Reggio Emilia); Paolo Burgio (University of Modena and Reggio Emilia); Jürgen Becker (Karlsruher Institut für Technologie)
14:00	#302 **WARP - A Runtime Wrapper Architecture for Task and Data Parallel Workloads** Ananda Biswas, Manish Manepalli and Akhilesh Tyagi (Iowa State University)

A12: Testing, Security, and Trust in Embedded Multicore/Manycore Systems – II

14:30–15:30 · Room A · Chair: TBC · Co-chair: Murali Shankar Dulam (JPMorgan Chase & Co.)

14:30	#222 **Fortified-Edge 6.0: Adversarial Analysis and Defense of Machine-Learning-Assisted PUF Authentication Systems** Jayaditya Vetsa and Sai Venkat Saketh Veerapaneni (University of Texas at Austin); Seema Gangaiah Aarella (Austin College & University of North Texas); Naga Surya Kamala Dattatreya Pasupuleti, Narender Reddy Bitla and Murali Shankar Dulam (JPMorgan Chase)
14:45	#203 **An ESP32 SoftAP Testbed for Authorized Wi-Fi Security Evaluation Under Single-Radio Constraints** Unais Ali and Jared Oluoch (Eastern Michigan University)
15:00	#319 **Large-Language-Model-Aided Intent Verification via Grounded Obligation Models** Surinder Sood (University of Manchester & ARM); John Goodacre (The university of manchester); Lucas Cordeiro (University of Manchester)
15:15	#52 **IGPO-SoC: Identity-Governed Privacy Orchestration for AI Acceleration on Embedded Multicore Systems-on-Chip** Jovita Nsoh (University of Houston & Google)

B12: Multicore SoCs for Cyber-Physical and Autonomous Systems – I

14:30–15:30 · Room B · Chair: Jani Babu Shaik (Shanghai Jiao Tong University) · Co-chair: Nachiappan Chockalingam (Meta)

14:30	#308 **Lightweight Visual SLAM for Nano-Drones with a Multi-Core RISC-V SoC** Hiroto Sugai (Tsukuba University); Keisuke Sugiura (University of Tsukuba); Yoshiki Yamaguchi (University of Tsukuba & Kumamoto University); Kentaro Tanaka (NTT Corporation); Toshihito Fujiwara (NTT & Access Network Service Systems Laboratories); Tatsuya Fukui (NTT Corporation & Access Network Service Systems Laboratories); Keita Takahashi (NTT)
14:45	#275 **Real-Time Vision Guided Walking Control for Humanoid Robots Using Detection and Tracking** Zhishang Wang, Hiromu Nagai and Khanh N. Dang (University of Aizu)
15:00	#129 **LAS-LiDAR: A Modular Linear LiDAR Architecture for Embedded Passage Monitoring** Wided Hammedi (Orange); Franck Roudet (Orange Labs); David Excoffier (Orange Research)
15:15	#281 **A Minimal Fixed-Function Triangle Rasterization Pipeline: Edge-Function Rasterization and Incremental Depth Testing on FPGA** Jiaqi Chen and Teo Tee Hui (Singapore University of Technology and Design); Chung-Yi Li (Chang Gung University); Chiang Liang Kok (The University of Newcastle Australia)

A13: S-Session 2: Emerging Machine Learning and Deep Learning Models: Theory and Applications

15:50–16:50 · Room A · Chair: TBC · Co-chair: Md Farhadur Reza (Eastern Illinois University)

15:50	#122 **Personalized Ontology-Driven Reasoning for Depression Detection on Social Media via Large Language Models** Zheqi Shen (The university of Aizu); Incheon Paik (The University of Aizu)
16:05	#127 **Formalizing Ethical Adaptation: A PEFT Framework with Rubric-Based Evaluation for LLM** Kumuduni Ranasinghe and Rumesh Weerakoon (University of Aizu); Incheon Paik (The University of Aizu)
16:20	#165 **A Diffusion-Augmented 3D Convolutional Framework for Multi-Class Dementia Screening** Md Farhadur Reza (Eastern Illinois University)
16:35	#205 **Dependency-Aware Thread Optimization in Multicore Systems** Ravi Meena (Malaviya National Institute of Technology Jaipur); Arjun Chaurasiya (Malaviya National Institute of Technology, Jaipur); Mushtaq Ahmed (Malaviya National Institute of Technology Jaipur INDIA)

B13: EmbodiCore Global Summit on Embodied AI, Collaborative Humanoid, and Distributed Robotic Computing

15:50–16:50 · Room B · Chair: TBC · Co-chair: Tejas Pravinbhai Patel (Amazon)

15:50	#290 **Design and Pipelined Implementation of an Artificial Neural Network for XOR Logic** Yihang Liu and Teo Tee Hui (Singapore University of Technology and Design)
16:05	#247 **A Parameter Sensitivity-Based Secure Audio Encryption Framework for Multimedia Communications** Adel Nadhem Naeem (Shatt Al-Arab University College); Ali Abdulqader Bin-Salem (Universiti Malaysia Sabah); Mahmood A. Al-Shareeda (Southern Technical University)
16:20	#266 **DT-NHURO: A Real-Time Digital Twin Framework for Bidirectional Control and Actuator-State Monitoring of a Neuromorphic Humanoid Robot** Yerima Williams (The University of Aizu & Allegis Group/Woven by Toyota); Zhishang Wang and Khanh N. Dang (University of Aizu)
16:35	#298 **An Event-Driven Agentic AI Architecture for Autonomous Error Recovery and Self-Evolution in Goal-Oriented Embodied Warehouse Robots** Nagaraju Akkuledu Uppara and Gangadhara Raghu Kopparapu; Udaya Bhasker Mattupalli (Accenture); Ayaskant Pattnaik and ShravanKumar Arram; Pralav Prasun (N2 Services Inc)

Thursday, December 17, 2026

A14: Testing, Security, and Trust in Embedded Multicore/Manycore Systems – III

09:00–10:00 · Room A · Chair: Siva Kumar Chintham (LTM) · Co-chair: TBC

09:00	#311 **A Framework for Test Program Automatic Generation Based on Large Language Model** Yang Yue, Heshan Yu, Zhenyu Wang and Zouqin Wang (Tianjin University); Zhaohui Guo (School of Microelectronics, Tianjin University); Qiang Liu (Tianjin University)
09:15	#116 **Custom RISCV Instructions for Reducing Size of Software-Based Self-Test** Jad Al Halabi (Infineon Technologies AG); Endri Kaja (Infineon Technologies AG & Rheinland-Pfälzische Technische Universität Kaiserslautern-Landau); Ares Tahiraga, Florian Thienel and Wolfgang Ecker (Infineon Technologies AG)
09:30	#120 **Selectable PE-Level Safety Mechanisms for an Open-Source Chisel AI Accelerator** Felix Frombach (Karlsruher Institut für Technologie); Georgios Sotiropoulos, Tanja Harbaum and Juergen Becker (Karlsruhe Institute of Technology)
09:45	#321 **Structural-Guided LLM-Based Reverse Engineering Attack for HLS/RTL Obfuscation** Srinivasa Rao Dara (IDRBT & NITW); Dipanjan Roy (IDRBT Hyderabad); Ilaiah Kavati (National Institute of Technology Warangal)

B14: Machine Learning for Energy-Efficient and Reliable Manycore Systems

09:00–10:00 · Room B · Chair: Lichen Weng (Tenstorrent) · Co-chair: Md Farhadur Reza (Eastern Illinois University)

09:00	#255 **FIRE: Enhanced Fine-Tuning for Efficient Self-Repair of Permanent Hardware Failures in AI Systems** Yixuan Luo (University of Chicago); Yanjing Li (Northeastern University)
09:15	#276 **A Spike-Domain RRAM-CIM Drift Monitoring and Calibration Framework with Dual-Stage Neural Adaptation for Cough Detection** Keyi Yang and Zixuan Shen (Huazhong University of Science and Technology); Yingchen Ji and Haoran Wang (Peking University); Sunbin Deng (Huazhong University of Science and Technology); Yimao Cai and Zongwei Wang (Peking University); Wang Chao (Huazhong University of Science and Technology)
09:30	#301 **Transfer Limits of Static and Causal Readout Calibration in Memristor Crossbars** Jin Shi (University of Nottingham Malaysia); Nandha Kumar Thulasiraman (University of Nottingham); Haider Abbas F. Almurib (The University of Nottingham Malaysia Campus)
09:45	#286 **A Trainable and Resource-Efficient Quantum Support Vector Machine for NISQ Computers** Sohrab Sajadimanesh, Saad Bin Ahmed and Ehsan Atoofian (Lakehead University)

A15: Hardware Acceleration of AI on Embedded Edge SoCs – III

10:20–11:20 · Room A · Chair: TBC · Co-chair: Ehsan Atoofian (Lakehead University)

10:20	#317 **A Parameterized Decoder Architecture with One-hot Regime Extraction for Posit Arithmetic Units** Diksha Shekhawat (CSIR-Central Electronics Engineering Research Institute); Jugal Gandhi (Academy of Scientific and Innovative Research (AcSIR) & CSIR-Central Electronics Engineering Research Institute); Jai Gopal Pandey (CSIR-Central Electronics Engineering Research Institute, Pilani); Chandra Shekhar (Birla Institute of Technology and Science)
10:35	#212 **Shared-Exponent Cross-Group Accumulation for Efficient Group-Wise Quantized LLM Inference** Zhengpan Fei and Satoshi Kawakami (Kyushu University); Takumi Honda and Naoto Fukumoto (Fujitsu Limited); Koji Inoue (Kyushu University)
10:50	#289 **Adaptive Resource Allocation for Low-Latency LLM Serving in Dynamic Environments** Masayuki Usui (Tokyo University); Shinya Takamaeda-Yamazaki (The University of Tokyo & RIKEN)
11:05	#305 **Data Movement and Memory Visibility in Coupling a CNN Accelerator to a RISC-V Host** Foivos Paraskevas, Iuliia Topko and Jan-Luca Ganz (Karlsruher Institut für Technologie); Georgios Sotiropoulos (Karlsruhe Institute of Technology); Sakir Sezer (Queen's University Belfast & Nvidia); Jürgen Becker (Karlsruher Institut für Technologie)

B15: Heterogeneous Integration and Advanced On-Chip Interconnects

10:20–11:20 · Room B · Chair: Siddhesh Shirodker (Qualcomm Technologies) · Co-chair: Abdul Khadir Mahamed (New York University)

10:20	#296 **Open Chiplet Atlas® Architecture: A Layered Chiplet Interoperability Definition with an Adoption-Ready Reference Design** Lichen Weng, Zhimin Chen and Wei-Han Lien (Tenstorrent)
10:35	#312 **A Low-Latency BCH-FEC Architecture for XSR SerDes-Based Chiplet D2D Interfaces** Wang Wenyi, Jiaqing Xu, Ouyang Kuo, Qiang Wang and Lai Mingche (National University of Defense Technology)
10:50	#291 **Quality-Adaptive Region Selection with Admission Pruning for Heterogeneous Partially Reconfigurable NoCs** Nguyen Van Cuong (Industrial University of Ho Chi Minh City)
11:05	#324 **Predictable Fixed-Hop Routing in Rectangular Mesh NoCs** C V Sesha Sai Kumar (BITS Pilani, Hyderabad Campus & Optima Design Automation Ltd); Soumya J (BITS Pilani, Hyderabad Campus); Sri Parameswaran (University of Sydney)

A16: Design Methodologies for Embedded Multicore/Manycore SoCs – I

11:20–12:20 · Room A · Chair: Mohamed Badawy (Infineon Technologies AG & Technical University of Munich) · Co-chair: Ehsan Atoofian (Lakehead University)

11:20	#117 **End-to-End Design and Evaluation of an IOMMU-Enabled RISC-V Heterogeneous SoC Platform for TEE Secure I/O** Yanqing Liu, Haocheng Xu, Hidetoshi Uranami, Akihiro Saiki and Keiji Kimura (Waseda University)
11:35	#217 **Design and FPGA Implementation of the RISC-V Advanced Interrupt Architecture for a Linux-Capable Multicore CVA6 SoC** Xinyuan Fu, Akihiro Saiki and Keiji Kimura (Waseda University)
11:50	#314 **MOSAIC-SoC: A Configuration-Driven Generator for Heterogeneous Multi-Core RISC-V Systems-on-Chip** Miloudi Adel Hani (Université de Blida); Taouinar Abdelbasset (University of Blida 1 & CDTA); Kheir Eddine Yassine Hamzi (Université de Blida); Nouma Izeboudjen (CDTA); Hamida Bougherira (Université de Blida I & Laboratoire LATSI); Nadjia Benblidia (Blida 1 university)
12:05	#254 **SimRV: An Explainable RISC-V Full-System Simulator for Architecture Education and Hardware/Software Codesign** Lennart Trunk and Kenji Kise (Institute of Science Tokyo)

B16: Hardware Acceleration of AI on Embedded Edge SoCs – IV

11:20–12:20 · Room B · Chair: Lichen Weng (Tenstorrent) · Co-chair: Krishna Suman Dara (HPE)

11:20	#124 **Compact RISC-V Packed-Vector and Matrix Custom Instructions for edge-AI Kernels** Kehan Peng, Rajesh C Panicker and Enming Xu (National University of Singapore)
11:35	#318 **Lightweight 3×3 Depthwise Acceleration with Sliding-Window Reuse in a RISC-V Custom Function Unit for INT8 MobileNetV2** Kasunya Himani, Mindi Rebeka, Sasmitha Jayasinghe and Stephan Balasuriya (University of Moratuwa); Chathuranga Hettiarachchi (University of Moratuwa & Nanyang Technological University)
11:50	#213 **MCU-Compatible Recurrent Neural Inference for Embedded AHRS** Qingshan Shan (Ningbo Intelligent Equipment Research Institute Co. Ltd. & School of Artificial Intelligence, Ningbo University of Finance & Economics)
12:05	#157 **An Efficient QML Simulator with Programmable Interconnection and Unified Operator Fusion** Zhengke Li (School of Integrated Circuits, Sun Yat-Sen University); Qiwei Dong (Nanjing University); Haolu Xie (School of Integrated Circuits, Sun Yat-Sen University); Wendong Mao and Zhongfeng Wang (Sun Yat-sen University)

Venue, Travel and Accommodation

Conference venue

Shanghai Jiao Tong University (Xuhui Campus)
KoGuan School of Law
1954 Huashan Road, Xuhui District, Shanghai
上海市徐汇区华山路 1954 号（上海交通大学徐汇校区）
Entrance: Gate 1 (1 号门)
Google Maps: maps.app.goo.gl/aPN72B4rCP9pksZUA
Baidu Maps: j.map.baidu.com/20/CA

Nearest metro station

Jiao Tong University Station (交通大学站), Exit 2 — Metro Lines 10 and 11
From Exit 2: turn left onto Huaihai West Road, then right onto Huashan Road. Gate 1 is about a 5-minute walk.
By taxi / DiDi: set the destination to “Shanghai Jiao Tong University Xuhui Campus – Gate 1” (上海交通大学徐汇校区–1 号门).

From Shanghai Hongqiao Airport (SHA) / Hongqiao Railway Station

Take Metro Line 10 directly to Jiao Tong University Station, Exit 2.
No transfer needed.

From Shanghai Pudong International Airport (PVG)

Take Metro Line 2 to Jiangsu Road Station, transfer to Line 11, and get off at Jiao Tong University Station, Exit 2.
A taxi or DiDi is also available from the airport taxi stand.

Accommodation

Recommended hotel: Crowne Plaza Shanghai
400 Panyu Road, Changning District, Shanghai
About 500 m from Metro Lines 10 and 11.
Group rates may be available; please contact the organizers.

Visa and invitation letters

Please check the visa requirements for your trip as early as possible; they depend on your nationality, length of stay and purpose of travel.
Invitation letters are issued only to participants who have completed full registration and payment. Contact: mcsoc.forum@gmail.com
An invitation letter does not guarantee visa approval.

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